CE5HL7XXM1Q - High Input Very-Low IQ 300mA LDO

General Description

CE5HL7XXM1Q series are the high input very low I_Q 300mA LDO with enable function that operates from 1.8V~15V. The very-low consumption of type 3.0μA ensures long battery life and dynamic transient boost feature improves device transient response for wireless communication applications. It has power-good feature especially in automotive applications.

CE5HL7XXM1Q series are offered ESOP8 package and support ambient temperature Range of -40°C to 125°C

Features

- Wide Input Voltage Range: 2.8V to 60V
- Up to 300mA Load Current
- Very low I_Q: 3.0μA
- Fixed Output Voltage are 1.8V, 3.0V, 3.3V, 3.6V, 5.0V, 8.0V, 12V, etc
- Low dropout: 1200mV @ 300mA / V_{OUT} = 3.0V
- Excellent Load/Line Transient Response
- High Ripple Rejection: 75dB at 1KHz
- Automotive AEC-Q100 Grade 1 Qualified
  -- Ambient Temperature Range of -40°C to 125°C
  -- ESD HBM 4KV PASS
  -- ESD CDM 1.5KV PASS
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
CE5HL7XXM1Q	ESOP8 (4.9mm × 6.0mm)	Tape and Reel, 4K/Reel	3

Device information

CE 5HL7 XX M1 Q

XX Output Voltage		**M1** Package		**Q** AEC-Q100 Qualified	
XX	X.XV Output Voltage For example, 33 is 3.3V output	M1	ESOP8	Q	With AEC-Q100 Qualified

Applications

- Automotive Constant-Voltage Power Supply
- Automotive Infotainment and Cluster
- Automotive Power Supply for Body Electronics and Lighting

Pin Configuration

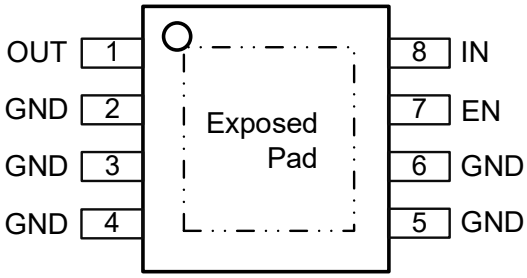


Figure1. Pin Configuration

Pin Function

Pin No. ESOP8	Pin Name	Pin Function
1	OUT	Output Pin.
2,3,4,5,6	GND	Ground.
7	EN	Enable Control Input, Active
8	IN	Supply Input Pin.

Block Diagram

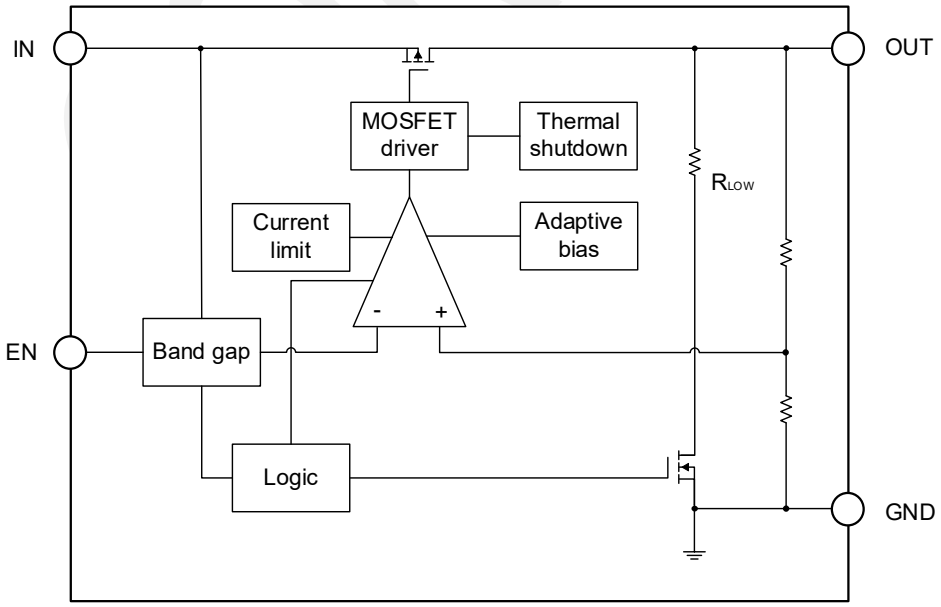


Figure2. Block Diagram

Functional Description

Input Capacitor

A 1μF~10μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Enable

The CE5HL7XXM1Q delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Dropout Voltage

The CE5HL7XXM1Q uses a PMOS pass transistor to achieve low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DROP} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} - V_{OUT}) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled.

Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} - V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 150°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 150°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA} is layout dependent. The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance(θ_{JA}).

Current-Limit Protection

The CE5HL7XXM1Q provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

Absolute Maximum Ratings

Symbol	Parameters	Value	Unit
V_{IN} (1)	Input Voltage	-0.3~70	V
V_{OUT}	Output Voltage	-0.3~20	V
V_{EN}	Chip Enable Input	-0.3~70	V
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65~150	°C
V_{ESD} (2)	HBM Capability	±4000	V
	CDM Capability	±1500	V
I_{LU} (2)	Latch up Current Maximum Rating	±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.

Note2. This device series incorporates ESD protection and is tested by the following methods:

HBM tested per AEC-Q100-002(JEDEC JS-001);

CDM tested per AEC-Q100-011(JEDEC JS-002);

Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	ESOP8	Thermal Characteristics, Thermal Resistance, Junction-to-Air	50	°C/W
P_D		Maximum Power Dissipate @ 25°C	2.5	W

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	2.8 to 60	V
I_{OUT}	Output Current	0 to 300	mA
T_A	Operating Ambient Temperature	-40 to 125	°C
C_{IN}	Effective Input Ceramic Capacitor Value	1 to 10	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Electrical Characteristics

(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage (3)		2.8		60	V
V_{OUT}	Output Voltage	T_A = 25°C	-2%		2%	V
I_Q	Quiescent Current	I_{OUT} = 0mA		3.0	10.0	μA
I_{Q_OFF}	Standby Current	V_{EN} = 0V		0.1	3	μA
Reg_{LINE}	Line Regulation (6)	V_{IN} = V_{OUT} + 2V to 60V, I_{OUT} = 10mA		0.02	0.2	%/V
Reg_{LOAD}	Load Regulation (6)	1mA ≤ I_{OUT} ≤ 300mA, V_{IN} = V_{OUT} + 2V		20	200	mV
V_{DROP}	Dropout Voltage I_{OUT}=300mA (4) (6)	V_{OUT} = 1.8V		1550	2150	mV
		V_{OUT} = 3.0V		1350	1950	
		V_{OUT} = 5.0V		1280	1850	
		V_{OUT} = 12V		1170	1750	
I_{LMT}	Current Limit	V_{IN} = V_{OUT} + 2V	300	450		mA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”			0.5	V
I_{EN}	EN Pin Current	V_{EN} = 0~60V		1		μA
PSRR	Power Supply Rejection Ratio (5)	f = 1kHz, V_{IN} = V_{OUT} + 2V I_{OUT} = 20mA		50		dB
e_N	Output Noise Voltage (5)	I_{OUT} = 1mA, C_{OUT} = 1μF, f = 10Hz to 100KHz		50* V_{OUT}		μVrms
T_{TSD}	Thermal Shutdown Temperature (5)	Temperature Increasing from T_A = 25°C		155		°C
T_{HYS}	Thermal Shutdown Hysteresis (5)	Temperature Falling from T_{TSD}		30		°C

Note3. Here V_{IN} means internal circuit can work normal. If V_{IN} < V_{OUT}, Output voltage follows V_{IN}(I_{OUT} = 1mA), circuit is safety.

Note4. V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} + $V_{DROPMAX}$ with 300mA output current.

Note5. Guaranteed by design and characterization. not a FT item.

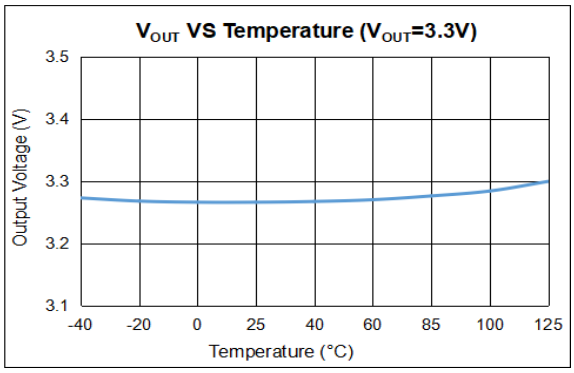
Note6: At high temperatures, the maximum load current can be calculated according to the following formula：

$$I_{OUT\_MAX} = (T_J - T_A) / R_{\theta JA} / (V_{IN} - V_{OUT})$$

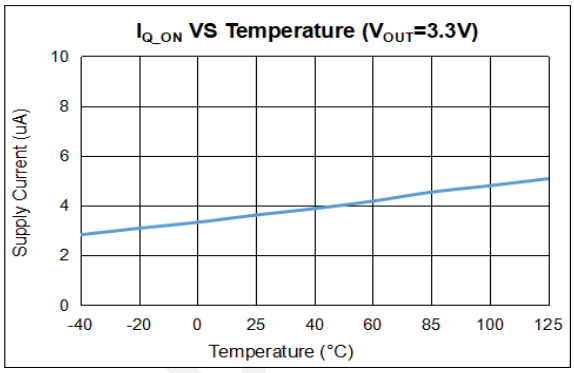
Typical Characteristics

VOLTAGE VERSION 3.3V

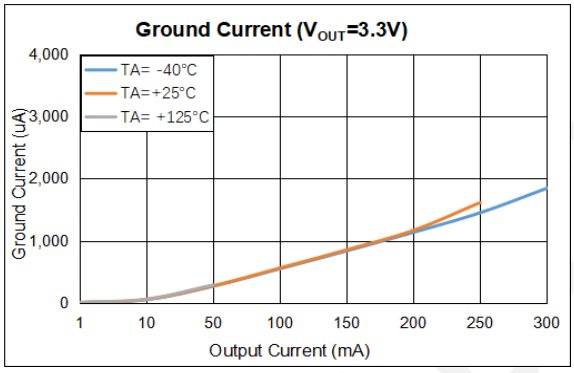
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.)



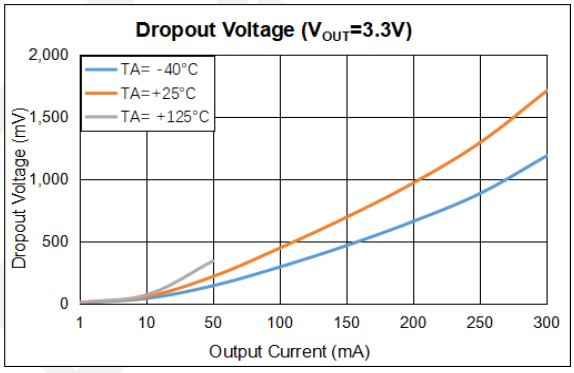
Output Voltage VS Temperature



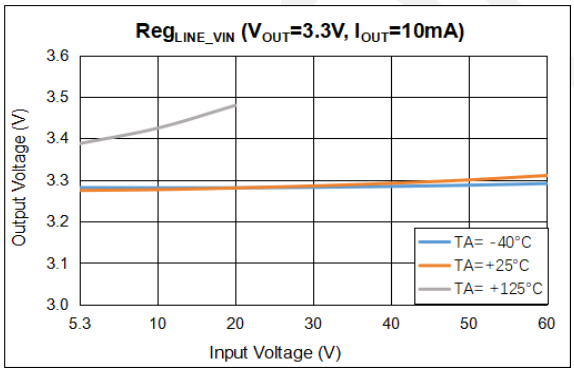
Quiescent Current VS Temperature



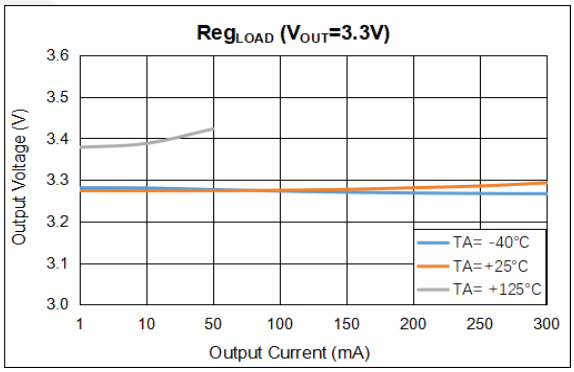
Ground Current VS Output Current



Dropout Voltage VS Output Current



Output Voltage VS Input Voltage

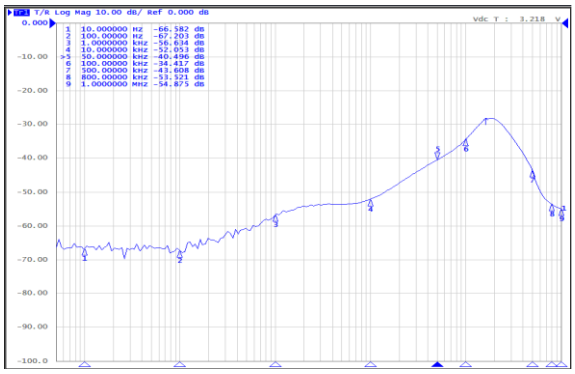


Output Voltage VS Output Current

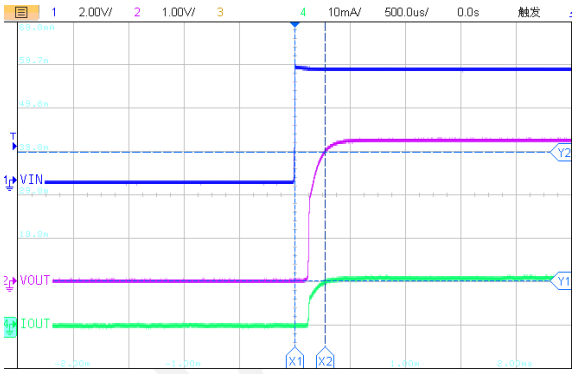
Typical Characteristics(Continued)

VOLTAGE VERSION 3.3V

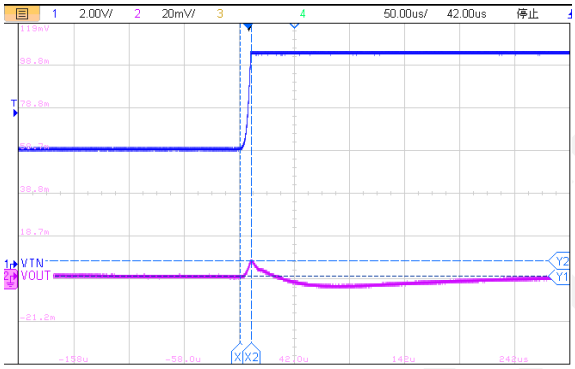
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.)



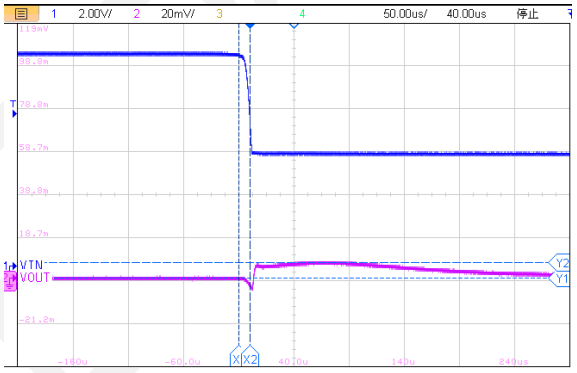
PSRR VS Output Current



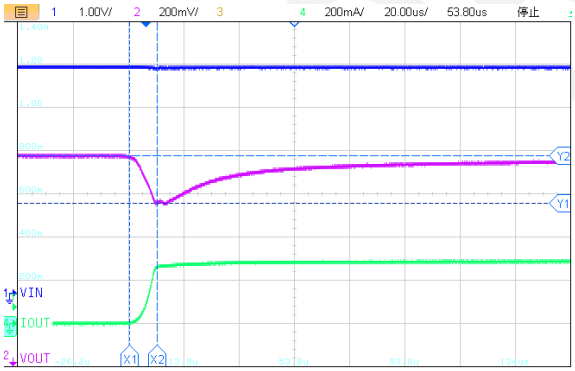
T_{ON}(I_{OUT} = 10mA)



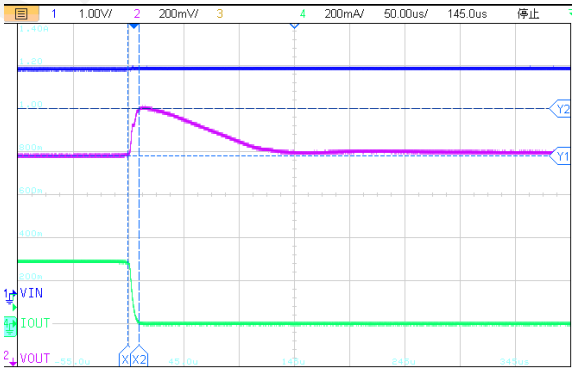
Input Transient(7~15V t = 10μs 10mA)



Input Transient(15~7V t = 10μs 10mA)



Load Transient(1mA~300mA t = 10μs)



Load Transient(300mA~1mA t = 10μs)

Application Circuits

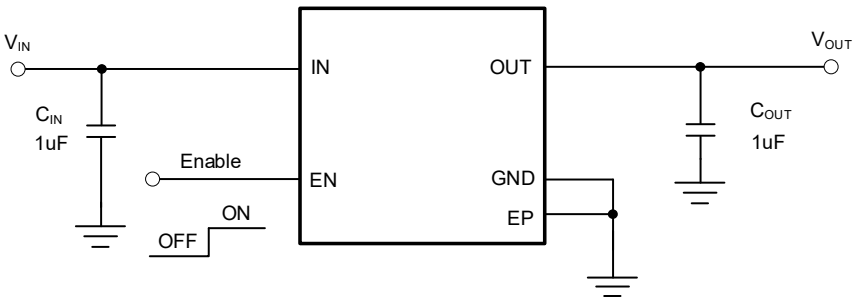


Figure3. Application Circuits

Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Do not place a thermal via directly beneath the thermal pad. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

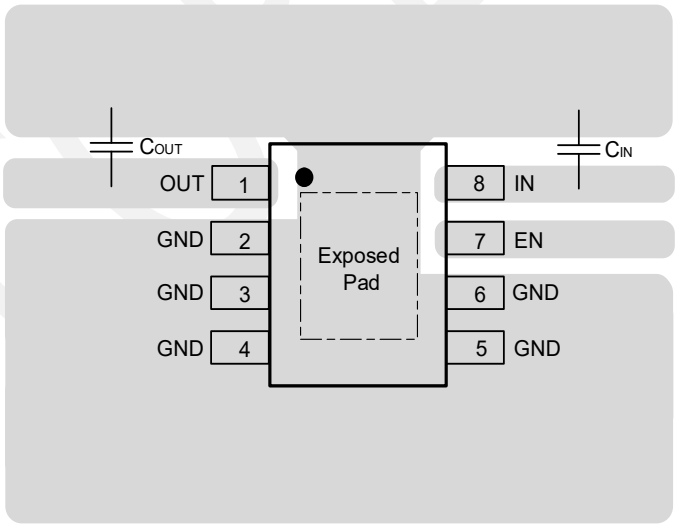
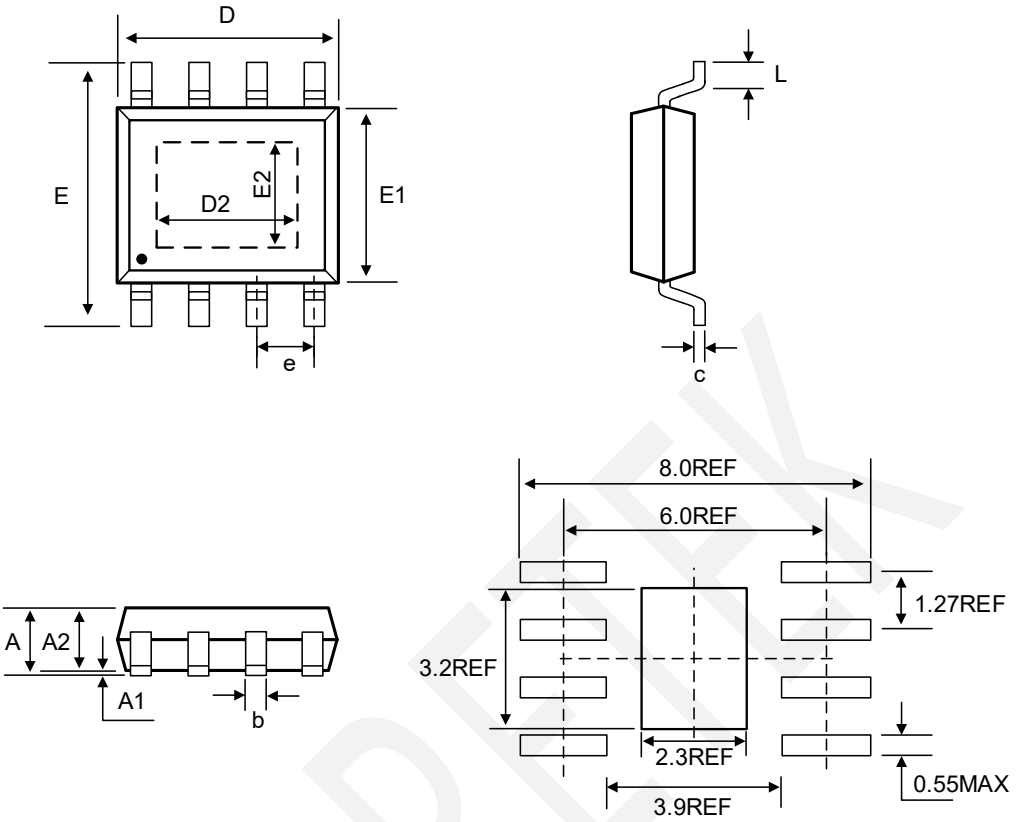


Figure4. PCB Layout Guide

Package Dimension

ESOP8



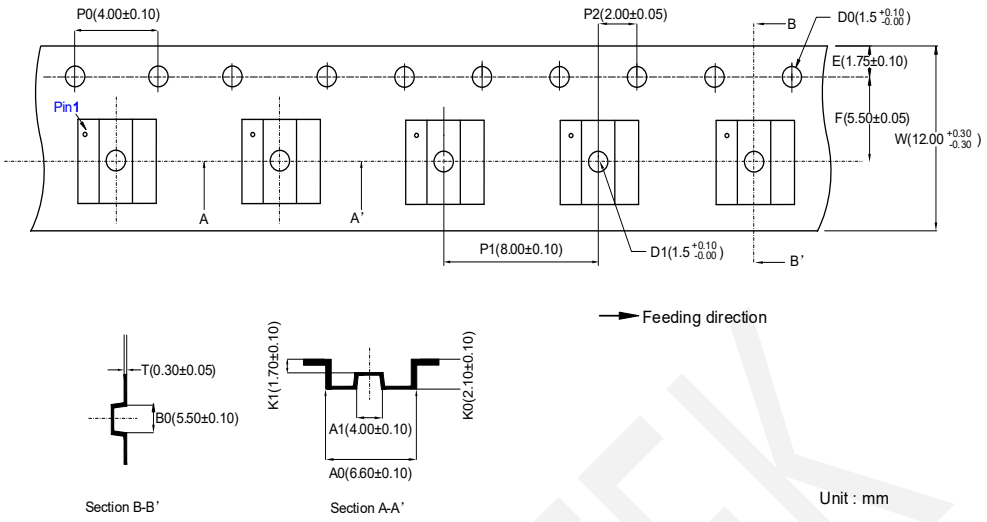
COMMON DIMENSIONS

(Unit: mm)

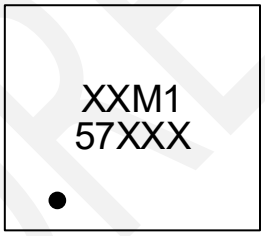
SYMBOL	MIN	NOM	MAX
A	-	-	1.90
A1	0.00	-	0.30
A2	1.20	1.40	1.60
b	0.35	-	0.51
c	0.15	-	0.27
D	4.70	4.90	5.10
E	5.80	6.00	6.20
D2	3.00	3.25	3.50
E1	3.70	3.90	4.10
E2	2.10	2.30	2.50
e	1.27BSC		
L	0.35	0.60	0.85

Tape Dimension

ESOP8



Marking Information



XXM1 = Output Version, e.g. 18M1: 1.8V

57XXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-06-17	Preliminary Version	Liu xiaomin, Wu han	Liu xiaomin	Liu jiaying
1.0	2023-10-07	Official Version	Peng junjie	Liu xiaomin	Liu jiaying