CE81D342VQ - 3.4V to 40V Input, 3.5A Step-Down Regulator

General Description

The CE81D342VQ is an easy-to-use, synchronous, step-down DC/DC converter designed for rugged automotive applications. It provides 3.5A output with current mode control for fast loop response and easy compensation. The wide 3.4V to 40V input range accommodates a variety of step-down applications, including those in an automotive input environment. 20μA operational quiescent current allows use in battery-powered applications.

High power conversion efficiency over a wide load range is achieved by scaling down the switching frequency at light load condition to reduce the switching and gate driving losses. The soft start function helps prevent inductor current run away during startup and thermal shutdown provides reliable, fault tolerant operation. In some applications, such as AM radio and ADSL applications, in which the device is sensitive to frequency band, the CE81D342VQ can avoid the related EMI problem by setting the frequency up to 2.2MHz.

The CE81D342VQ is available in TSSOP16 (Exposed Pad) package.

Features

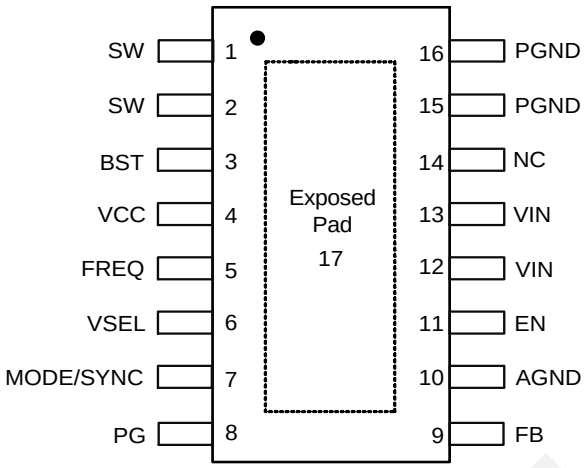
- 3.5A Converters Integrated 90mΩ High Side MOSFET and 60mΩ Low Side MOSFET
- 20uA Quiescent Current When No Switching in Automatic PFM/PWM Mode
- Wide 3.4V to 40V Operating Input Range
- 200KHz to 2.2MHz Switching Frequency Programmed By External Resistor
- MODE/SYNC: Set Force PWM Mode or Automatic PFM/PWM Mode
  Or Synchronize External 200KHz to 2.2MHz Clock
- Spread spectrum frequency modulation to Minimize EMI
- VSEL set 5V or 3.3V V_{OUT} and FB set Adjustable 0.8V to 20V V_{OUT}
- Power Good Indication
- Internal Soft-Start
- Automotive AEC-Q100 Grade 1 Qualified, Operate -40 °C to +125 °C ambient temperature range.
- Part No. and Package

Part No.	Package
CE81D342VQ	TSSOP16

Application

- Automotive Battery Powered Supplies (Cluster Panels, Car Multimedia)
- Automotive (body, audio system, navigation system, etc).
- Industrial / Consumer Supplies
- Other electronic equipment Digital

Pin Configuration



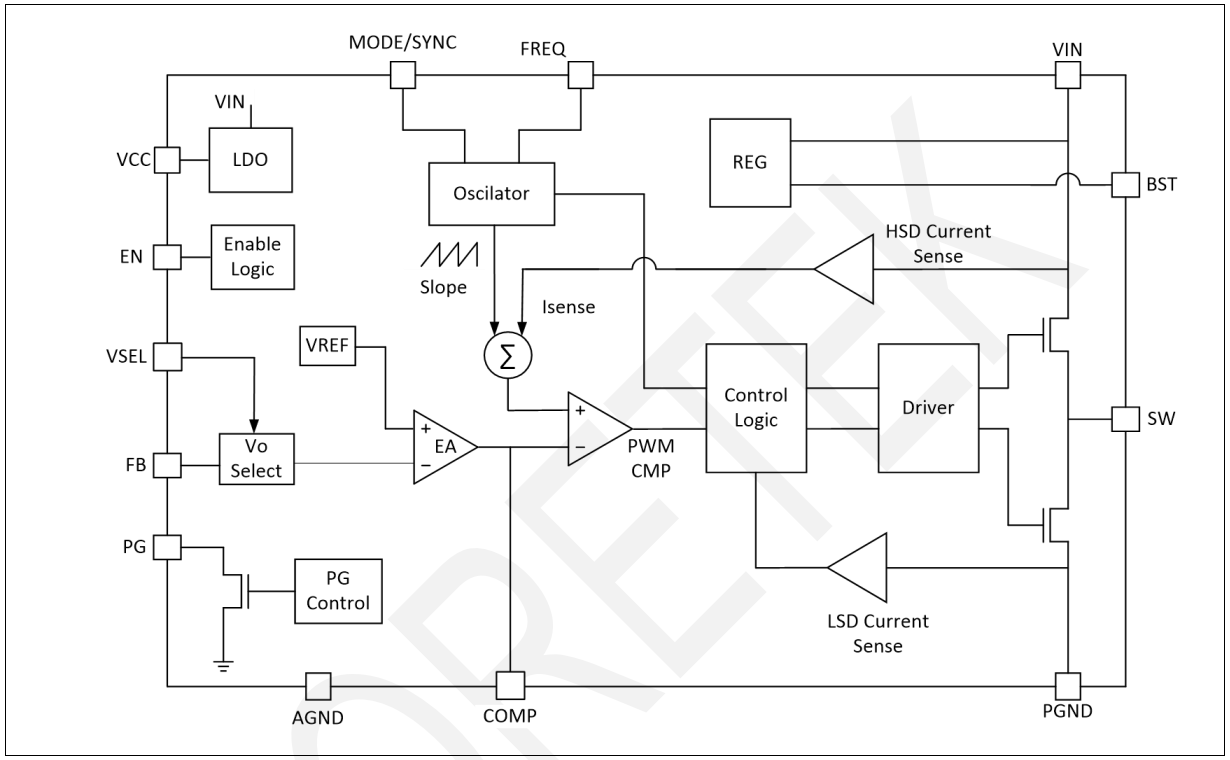
CE81D342VQ
Top View

Pin Function

Pin Name	Pin No.	Description
SW	1,2	Switch Node. This node is connected to the source of high-side power FET and drain of low-side power FET.
BST	3	Bootstrap. This is the positive power supply for the internal floating high-side MOSFET driver. Connect a bypass capacitor between this pin and SW pin.
VCC	4	The output of internal LDO. Connect 1uF capacitor from this pin to PGND.
FREQ	5	Switching Frequency Program Input. Connect a resistor from this pin to ground to set the switching frequency.
VSEL	6	Output voltage select input. Tie to VCC for 5V output or to AGND for 3.3V output; connect a 10kΩ for an adjustable output. Don't let it float.
MODE /SYNC	7	Mode selection and synchronization input pin. Leave it floating for force PWM mode, tie it to AGND for automatic PFM/PWM mode, or supply an external synchronizing clock to this input.
PG	8	Power Good output pin. It will go from logic low to logic high (through an external pull-up resistor) once the output voltage is within 93% of the nominal set point
FB	9	Feedback. This is the input to the error amplifier. The output voltage is set by a resistive divider connected between the output and GND which scales down V_{OUT} equal to the internal 0.8V reference.
AGND	10	Analog ground. It should be connected as close as possible to the output capacitor to shorten the high current switch paths.
EN	11	Enable Input. Pulling this pin below the specified threshold shuts the chip down. Pulling it up above the specified threshold or leaving it floating enables the chip.

VIN	12,13	Input Supply. A decoupling capacitor to ground must be placed close to this pin to minimize switching spikes.
NC	14	No internal connection to device
PGND	15,16	Power ground
Exposed Pad	17	Exposed pad. The exposed pad is internally unconnected and must be soldered to a large PGND plane. Connect this PGND plane to other layers with thermal vias to help dissipate heat from the device.

Block Diagram



Functional Description

Overview

The CE81D342VQ is a variable frequency, non-synchronous, step-down switching regulator with an integrated high-side high voltage power MOSFET. It provides a single highly efficient solution with current mode control for fast loop response and easy compensation. It features a wide input voltage range, internal soft-start control and precision current limiting. Its very low operational quiescent current makes it suitable for battery powered applications.

PWM Control

At moderate to high output current, the CE81D342VQ operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off for at least 100ns before the next cycle starts. If in one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET remains on, saving a turn-off operation.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 4V. When it is lower than the internal reference (VREF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than VREF, VREF regains control.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than its upper threshold, it shuts down the whole chip. When the temperature is lower than its lower threshold, the chip is enabled again.

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET OFF for about 50μs to blank the startup glitches. When the internal soft-start block is enabled, it first holds its SS output low to ensure the remaining circuitries are ready and then slowly ramps up.

Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, power MOSFET is turned off first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down.

FPWM Operation

Leaving MODE pin floating can force the converter work in force PWM mode (FPWM), and tie MODE pin to GND can make it work in automatic PFM/PWM mode. In PFM/PWM mode, when load is heavy or medium, it works in PWM mode. When the load it light, it works in PFM mode in order to achieve high efficiency.

Synchronizing External Clock

When a valid clock signal is applied on the MODE input, the switching frequency is locked to the external clock. The switching frequency is no longer determined by the resistor R_{FREQ} between pin FREQ and GND. In this scenario the device mode is also FPWM. The allowed frequency range of external clock is from 200KHz to 2.2MHz. The mode can be also changed dynamically by the system.

Spread Spectrum

The CE81D342VQ uses a triangle waveform to spread the switching frequency with ±10% of normal frequency. The frequency of the triangle waveform is typically 0.4% of the switching frequency. For example, if the normal switching frequency is programmed to 2.2MHz, the spread spectrum function modulates the switching frequency in the range of 1.98MHz to 2.42MHz in a triangle behavior with an 8.8KHz rate. The spread spectrum is only available while the converter is running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- An external clock is applied to the MODE pin.
- The device works in PFM operation at light load.

Programmable Oscillator

When there is no external clock signal at MODE pin, the switching frequency can be set by an external

resistor, R_{FREQ} from the FREQ pin to ground. The relationship between R_{FREQ} and switching frequency f_s refer to below Table 1.

Table 1. Programmable Oscillator

R_{FREQ} (kΩ)	f_S (MHz)
176kΩ	250KHz
88kΩ	500KHz
58.7kΩ	750KHz
44kΩ	1.0MHz
29.3kΩ	1.5MHz
20kΩ	2.2MHz

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors may also suffice.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Parameters		Min	Max	Unit
V_I	VIN,EN	-0.3	45	V
	VBST	-0.3	45	V
	SW	-2	V_{IN} +0.3	V
	VBST(VS SW)	-0.3	6.5	V
	VFB	-0.3	6.5	V
	All Other Pins	-0.3	6.5	V
V_{ESD}	Human Body Model (JEDEC JS-001)		±3000	V
	Charged Device Model (JESD22-C101)		±1000	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameters		MIN	MAX	Unit
V_{IN}	Supply Input Voltage Range		3.4	40	V
V_I	Input Voltage Range	VIN,EN	-0.1	36	
		VBST	-0.1	40	
		SW	-0.1	V_{IN}	
		VBST (VS SW)	-0.1	5.5	
		VFB	-0.1	5.5	
		All Other Pins	-0.1	5.5	
T_J	Operating Junction Temperature		-40	150	°C
T_A	Ambient Temperature		-40	125	°C

Electrical Characteristics

V_{IN} = 12V, T_A = –40°C to 125°C, (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Current						
I_{VIN}	Operating–non-switching Supply Current	V_{IN} current, EN = 5V,V_{FB} = 0.8V		18		μA
I_{VINSDN}	Shutdown supply current	V_{IN} current, EN = 0V		1.6	5	
Logic Threshold						
V_{ENH}	EN High-level Input Voltage		1.6			V
V_{ENL}	EN Low-level Input Voltage				0.8	
R_{EN}	EN Pin Resistance to GND	V_{EN} = 12V	200	320	600	kΩ
V_{FB} Voltage and Discharge Resistance						
V_{FBTH}						
	V_{FB} Threshold Voltage	4.5V < V_{IN}< 36V	784	800	816	mV
I_{VFB}	V_{FB} Input Current	V_{FB} = 0.8V			0.1	μA
MOSFET						
R_{DS_H}	High-side Switch Resistance	T_A = 25°C, V_{BST} – SW = 5V		90		mΩ
R_{DS_L}	Low-side Switch Resistance	T_A = 25°C, V_{IN} = 12V		60		mΩ
Current Limit						
I_{OCL}	Current Limit	DC current, V_{OUT} = 1.05V, L_1 = 2.2μH	4.0	4.5		A
Thermal Shutdown						
T_{SDN}	Thermal Shutdown Threshold(1)	Shutdown temperature		170		°C
		Hysteresis		30		
ON-Time Timer Control						
$t_{OFF(MIN)}$	Minimum off Time	V_{FB} = 0.5V		150		ns
Soft Start						
T_{SS}	Soft Start Time	Internal soft-start time		1.6		ms
Frequency						
F_{SW}	Switching Frequency	R_{FREQ} = 45kΩ	1.8	2.2		MHz
Output Under-voltage and Over-voltage Protection						
V_{UVP}	Output UVP Threshold	Hiccup detect (H > L)		60		%
T_{HICCUP_WAIT}	Hiccup on Time			6.4		ms
T_{HICCUP_RE}	Hiccup Time Before Restart			102		ms
UVLO						
V_{UVLO}	UVLO Threshold	Wake up V_{IN} voltage		3.4	3.5	V
		Shutdown V_{IN} voltage	3.0	3.1		
		Hysteresis V_{IN} voltage		0.3		

Note(1) Not production tested, design assurance.

Typical Characteristics

To be added

Application and Implementation

Note

CTK does not warrant its accuracy or completeness and Information in the following applications sections is not part of the CTK component specification. Customers should be responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

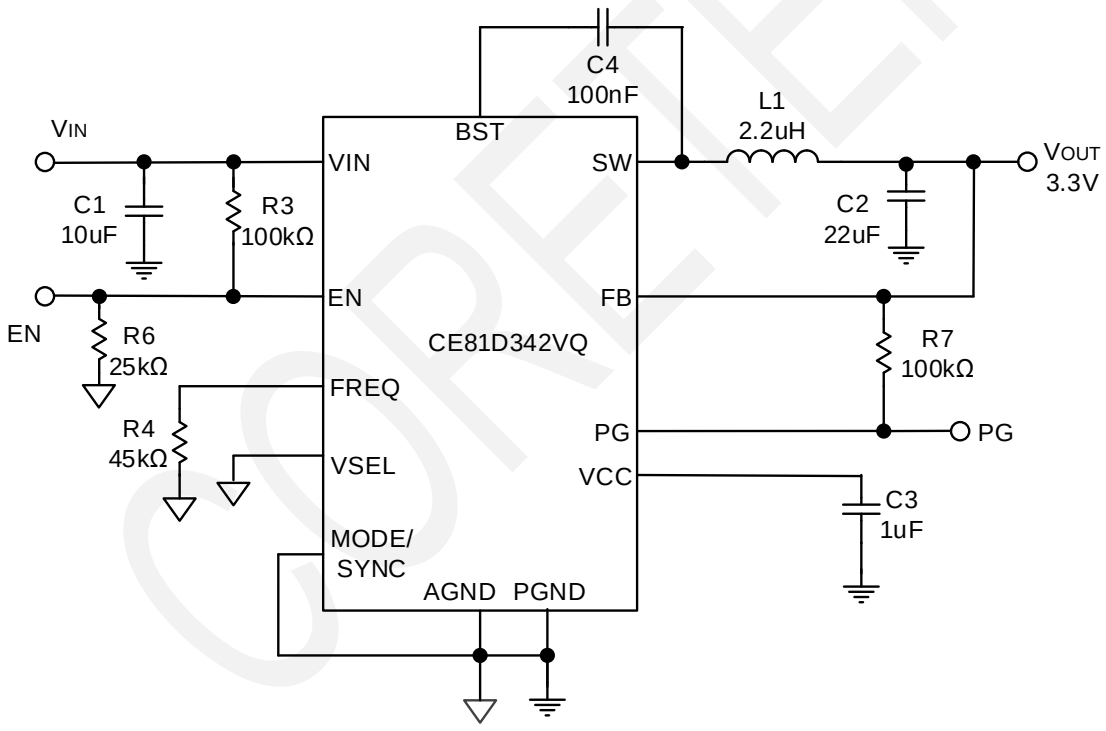
Application Information

CE81D342VQ is typical step-down DC-DC converter. It's typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3.5A. The following design procedure can be used to select component values for the CE81D342VQ.

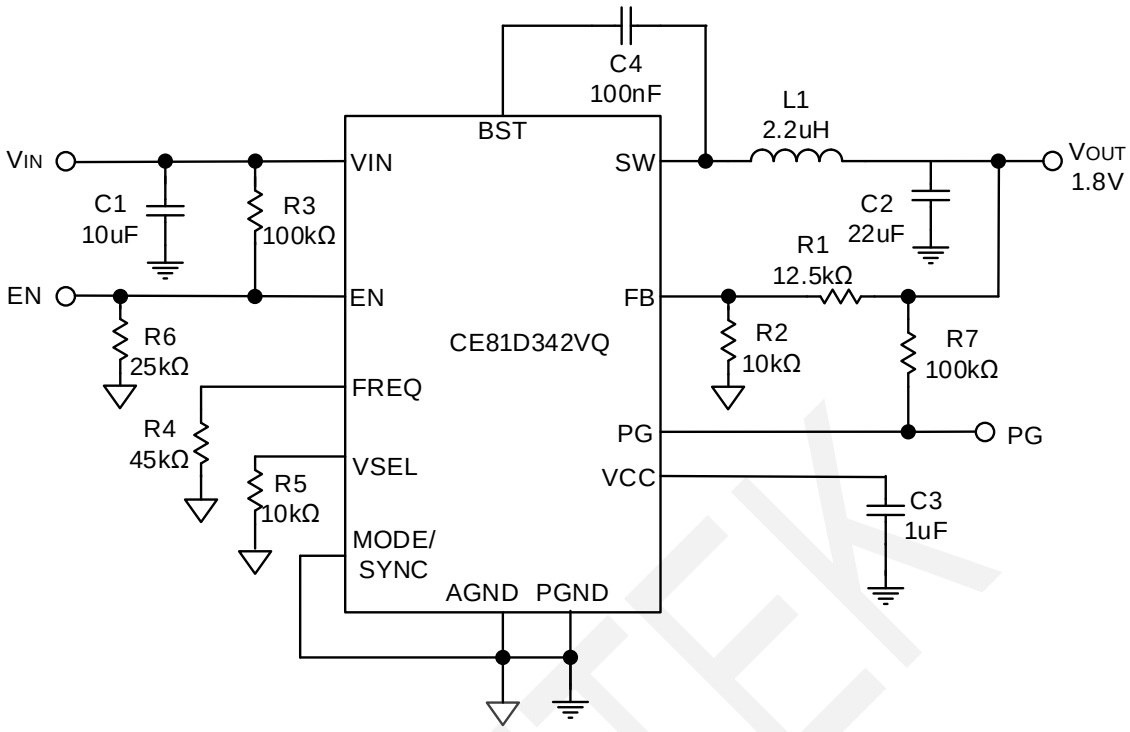
Typical Application

The application schematic below was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

The figure shows CE81D342VQ schematics.



VOUT = 3.3V converter schematics.



VOUT = 1.8V converter schematics

Detailed Design Procedure

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. CTK recommends using 1% tolerance or better divider resistors. Start by using Equation 1 to calculate VOUT.

If customers want to improve efficiency at very light loads，we recommend using larger value resistors. High value of resistor will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.8 \times (1 + \frac{R1}{R2}) \qquad (1)$$

Output Filter Selection

The LC filter used as the output filter has double pole at Equation 2:

$$f_p = \frac{1}{2\pi \sqrt{L_{OUT} \times C_{OUT}}} \qquad (2)$$

The overall loop gain is set by the output set-point resistor divider network and the internal gain of the device at low frequencies. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a －40dB per decade rate and the phase drops rapidly. The inductor and capacitor for the output filter should be selected is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit.

To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

Output Voltage (V)	R1 (kΩ)	R2 (kΩ)	L1 (μH)			C2 (μF)
			Min	Typ	Max	
1	2.5	10.0	1.5	2.2	4.7	20 to 68
1.05	3.125	10.0	1.5	2.2	4.7	20 to 68
1.2	5	10.0	1.5	2.2	4.7	20 to 68
1.5	8.75	10.0	1.5	2.2	4.7	20 to 68
1.8	12.5	10.0	1.5	2.2	4.7	20 to 68
2.5	21.25	10.0	2.2	2.2	4.7	20 to 68
3.3	31.25	10.0	2.2	2.2	4.7	20 to 68
5	52.5	10.0	3.3	3.3	4.7	20 to 68
6.5	71.25	10.0	3.3	3.3	4.7	20 to 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 3,Equation 4, and Equation 5. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$II_{p\text{-}p} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{sw}} \quad (3)$$

$$II_{peak} = I_O + \frac{II_{p\text{-}p}}{2} \quad (4)$$

$$I_{LO(RMS)} = \sqrt{I_O^{\,2} + \frac{1}{12} II_{P-P}^{\,2}} \quad (5)$$

For this design example, the calculated peak current is 3.5A and the calculated RMS current is 3.01A.

The inductor should be used with a peak current rating of 13A and an RMS current rating of 9A.

The capacitor value and ESR determines the amount of output voltage ripple. The ET81324 is intended for use with ceramic or other low ESR capacitors. We recommend using values range from 20uF to 68uF. Equation 6 determines the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{sw}} \quad (6)$$

Two 22μF output capacitors are used for this design. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286A and each output capacitor is rated for 4A.

Input Capacitor Selection

The CE81D342VQ requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. We recommend a ceramic capacitor over 10uF for the decoupling capacitor.

Bootstrap Capacitor Selection

A 0.1uF ceramic capacitor must be connected between the BST to SW pin for proper operation. We recommend using a ceramic capacitor.

Power Supply Recommendations

CE81D342VQ is designed to operate from input supply voltage in the range of 4.5V to 36V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is V_{OUT}/0.75.

Application Curves

To be added

Layout

Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance and better heat dissipation.

2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize-trace impedance.

3. Provide sufficient Vias for the input capacitor and output capacitor.

4. Keep the SW trace physically short and wide to minimize radiated emissions.

5. Do not allow switching current to flow under the device.

6. A separate VOUT path should be connected to the upper feedback resistor.

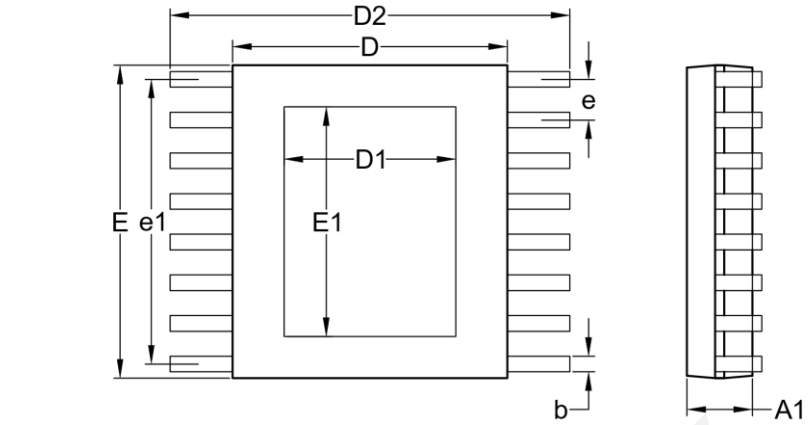
7. Make a Kelvin connection to the GND pin for the feedback path.

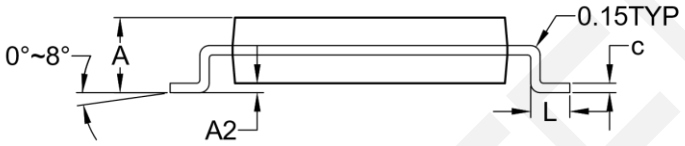
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably hasground shield.

9. The trace of the VFB node should be as small as possible to avoid noise coupling.

10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its-trace impedance.

TSSOP16





COMMON DIMENSIONS

(Unit: mm)

SYMBOL	MIN	NOM	MAX
A	—	—	1.20
A1	0.80	—	1.50
A2	0.05	—	0.15
b	0.19	—	0.30
c	0.09	—	0.20
D	4.30	4.40	4.50
D1	2.65	—	2.84
D2	6.25	—	6.55
E	4.90	5.00	5.10
E1	3.56	—	3.78
e	0.65 TYP		
e1	4.55 TYP		
L	0.45	—	0.75

Revision History and Checking Table

Version	Date	RevisionItem	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2025-12-27	Preliminary Version	Liu cong	Xielh	Shi Bo