CE81D340MQ - 4.5V to 36V Input, 3A Synchronous Step-Down Regulator

General Description

The CE81D340MQ is a highly integrated, internally compensated, 4.5 V to 36 V wide input voltage, 3 A output synchronous buck convertor.

The device is optimized to operate with minimum external component counts and also optimized to achieve

low standby current, with 64 μA (TYP) quiescent current and ultra-low 0.6 μA (TYP) shutdown current, they are well suited for battery powered systems to prolong battery life. Internal compensation allows quick and low component count design.Easy compensation and cycle-by-cycle current limit are obtained by peak current mode control.

CE81D340MQ can operate at fixed frequency with moderate or heavy load condition. In light load condition, the CE81D340MQ enters in the pulse frequency modulation (PFM) mode to improve high efficiency.

The EN/SYNC employs an enable divider to establish a precision threshold that simplifies UVLO adjustment, device on/off control and power sequencing. Thermal shutdown and output short-circuit protection (hiccup mode) are also provided.

CE81D340MQ is available in ESOP8 package and can operate over -40 °C to +125 °C ambient temperature range.

Features

- Wide Input Voltage Range: 4.5 V to 36 V
- 3A Converters Integrated 115 mΩ and 90 mΩ FET
- Output Voltage Range: V_{FBTH} to 24 V
- FB voltage is 0.8 V (TYP)
- Ultra-Low Shutdown Current:0.6 μA (TYP)
- PFM mode during light load operation
- 390 kHz Switching Frequency
- SYNC Input for External Switching Clock
- Start-up from Pre-Biased Output Voltage
- Peak Current Mode Control
- Cycle-by-Cycle Over-current Limit
- Hiccup-mode Over-current Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.5 ms (TYP)
- Automotive AEC-Q100 Grade 1 Qualified

- Operate over -40 °C to +125 °C ambient temperature range.

- ESD HBM ±2KV PASS

- ESD CDM ±1KV PASS

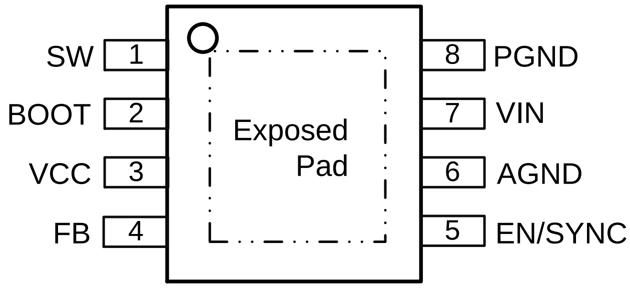
- Part No. and Package

Part No.	Package	MSL
CE81D340MQ	ESOP8 (4.9 mm × 6.0 mm)	3

Application

- Industrial Power Supplies
- Telecom and Datacom Systems
- Automotive Purpose Wide VIN Regulation

Pin Configuration



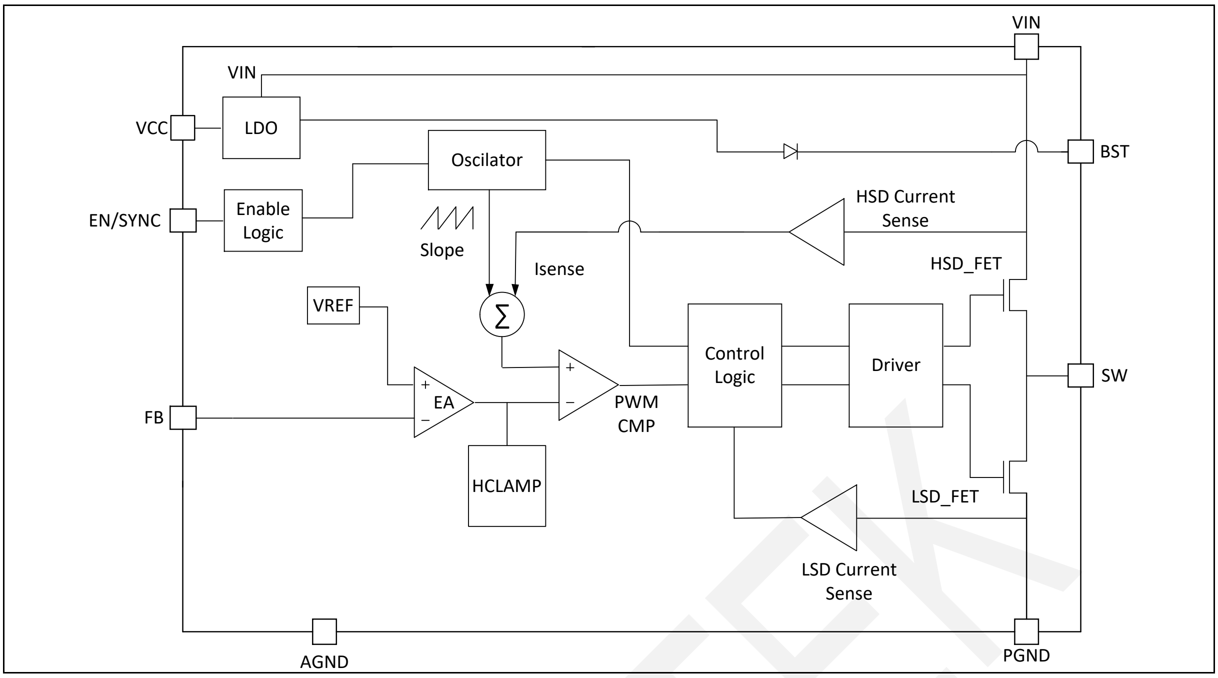
Top View

Pin Function

Pin Name	Pin No.	I/O	Description
SW	1	O	Switch node connection between low-side NFET and high-side NFET.
BOOT	2	O	Bootstrap Input. Bootstrap supply for high-side driver. Connect a 470nF ceramic capacitor between BOOT and SW pins.
VCC	3	O	LDO (Internal Bias) Output. This pin is provided for bypassing to AGND only. Never load VCC.
FB	4	I	Output voltage feedback pin. Connect to output voltage with feedback resistor divider.
EN/SYNC	5	I	Active High Enable and Synchronous Input. Do not float. EN: This pin can be connected to VIN pin via a resistor if the shutdown feature is not required or to a resistor divider to adjust UVLO threshold. SYNC: An external clock with positive pulses can be coupled to this pin by a small capacitor for synchronizing the internal switching oscillator.
AGND	6	-	Analog Ground. Reference for internal analog signals and logic. Connect it to system ground.
VIN	7	I	Power Supply Input Pin. Connect C_{IN} as close as possible between this pin and PGND pin.
PGND	8	-	Power Ground. It is internally connected to converter return. Returns of the CIN and COUT capacitors should be connected close to this pin. Connect to system ground, exposed pad and AGND together.
EP	-	-	Exposed Pad for heat dissipating, it is recommended to connect GND

Note: The Exposed Pad must be connect with GND on Printed Circuit Board.

Block Diagram



Functional Description

Overview

The CE81D340MQ are 3 A output synchronous Buck converters with internal compensation and peak current mode control. They can operate from an input voltage range of 4.5 V to 36 V. These devices need a few external components and provide an easy and small size power supply solution for industrial applications with good thermal performance. With 64 µA(TYP) quiescent current and 0.6 µA (TYP) shutdown current, they are also well suited for battery powered applications.

CE81D340MQ normally operate at fixed 390 kHz frequency in heavy load. At light load condition, the CE81D340MQ enters PFM mode to keep high efficiency.The normal frequency can be synchronized to an external clock between 200 kHz and 2.2 MHz.

Accurate EN input threshold and internal soft-start time (1.5 ms TYP) add more design flexibility to these devices.

Additional features such as thermal shutdown, input under-voltage lockout, cycle-by-cycle current limit, and short-circuit protection (hiccup mode) are also provided.

Switching Frequency and Current Mode Control

The basic waveforms of Buck synchronous converters are shown in Figure 1. The N-MOSFETs are used for high-side (HS) and low-side (LS) (synchronous rectifier) switches. The HS duty cycle ($D = t_{ON}/t_{SW}$) is controlled in closed loop to regulate and maintain the output voltage at a constant level. The switching period is $t_{SW}= 1/f_{SW}$, and the HS on-time is t_{ON}. When HS is turned on, the SW node voltage sharply rises towards V_{IN}, and the inductor current (I_L) starts ramping up with (V_{IN} -V_{OUT})/L slope. When HS is turned off, the LS is turned on after a very short dead time to avoid shoot-through, and I_L ramps down with -V_{OUT}/L slope. When the inductor current is continuous (either due to sufficient load), the output voltage is proportional to the input voltage and duty cycle ($V_{OUT} = D \times V_{IN}$) if component parasitics are ignored.

The output voltage is sensed by a resistor divider through FB pin and is regulated by feedback loop. This voltage is compared to an accurate reference and the voltage error signal is used as set point for an inner current loop that adjusts the peak inductor current. The input to the current loop is clamped to a fixed level to limit the maximum peak current and is compared to the actual peak current, sensed by the voltage drop across the HS switch to control the HS switch on-time. The loop internal compensation allows easy and stable design of the power supply with a few external elements for almost any output capacitor arrangement.

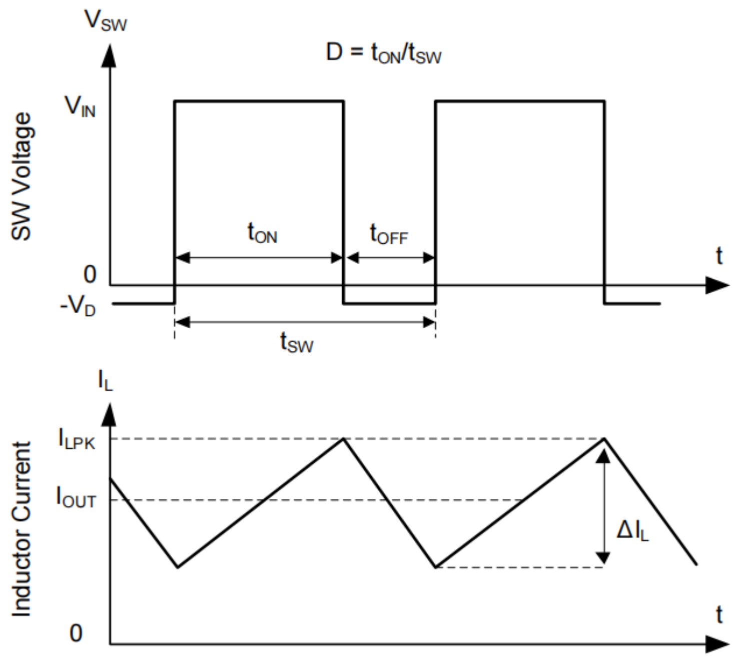


Figure 1.Converter Switching Waveforms in CCM

Pulse Frequency Modulation

The CE81D340MQ is designed with pulse frequency modulation mode to achieve high efficiency during light load condition. As the output current decreases from heavy load condition, the inductor current also deceases and eventually comes to zero, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side power FET is turned off when the zero inductor current is detected. As the load current further decreases the convertor enters into discontinuous conduction mode. The on-time is almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps efficiency high in light load condition. The transition point to the light load operation IOUT(LL) current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \qquad (1)$$

In PFM mode, each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the threshold voltage. As the output current decreases, the sleep time between switching pulses increases.

EN/SYNC Input

The EN/SYNC pin is an input and must not be left open. The simplest way to enable the device is to connect this pin to VIN pin via a resistor. This allows for self-startup of the CE81D340MQ when V_{IN} > V_{IN_UVLO}. This pin can also be used to turn the device on or off with logic or analog signals. If V_{EN} < 1.07 V (TYP), the device will shut down. Only if V_{EN} > 1.50 V (TYP) the device will start operation.

The system UVLO level can be increased accurately with a resistor divider(see Figure 2). This feature can be used for power supply sequencing which is required for proper power up of the system voltage rails. It can also be used as protection, such as preventing supply battery from depletion. Control of the enable input by logic signals may also be used for sequencing or protection.

The EN/SYNC pin can also be used to synchronize the internal oscillator to an AC coupled external clock (see Figure 3). The SW cycles synchronize to the rising edges of the clock. Synchronization range is from 200 kHz to 2.2 MHz. The clock signal peak-to-peak voltage must exceed 2.8 V to override the internal oscillator but must be kept below 5.5 V. Also the on and off pulse widths of the clock must be at least 100 ns (TYP). 3.3 V clock amplitude and CSYNC = 1 nF (coupling capacitor) should be sufficient for most designs. Keep the RENT||RENB near 100 kΩ range for stable syncing. The RENT is necessary for external syncing but the RENB is only needed for UVLO adjustment.

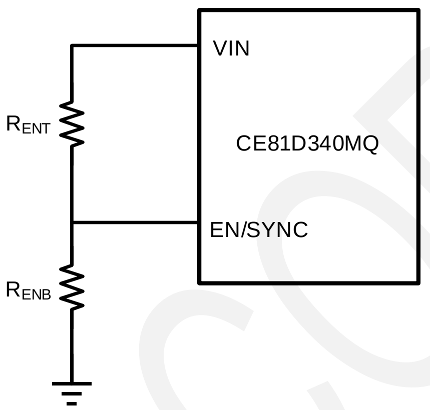


Figure 2. Changing the System UVLO

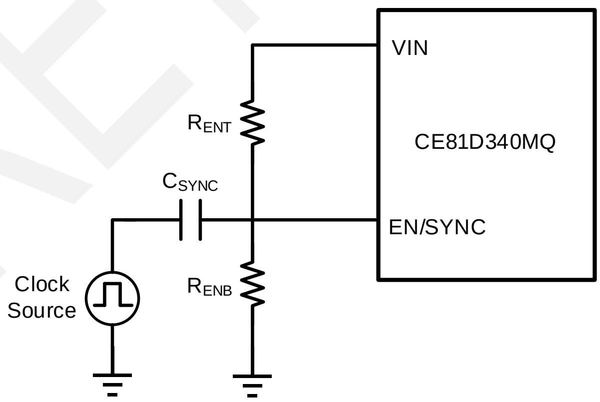


Figure 3. Synchronization to External Clock

BOOT (Bootstrap Voltage)

The gate driver of the HS N-MOSFET switch requires a voltage higher than V_{IN} that is present on its drain. A bootstrap voltage regulator is integrated to provide this voltage which is powered by bootstrapping through a small ceramic capacitor placed between the BOOT and SW pins. C_{BOOT} is charged in each cycle when the LS switch is turned on ($V_{SW} \approx 0$ V) and discharges to the boot regulator when the HS switch is turned on ($V_{SW} \approx V_{IN}$). A 0.47 μF ceramic capacitor with 16 V or higher rated voltage is recommended.

VCC Decoupling

The VCC pin is connected to the output of an LDO that is integrated in the device and provides a 5 V supply (nominal) for the internal circuitry and MOSFET drivers. It is intended for bypassing LDO output to ground and should not be loaded. A 2.2 μF to 10 μF stable ceramic capacitor rated for 16 V_{DC} or higher must be placed as close as possible to VCC pin and grounded to the exposed pad and ground pins. The device may be damaged if VCC pin is shorted to ground during operation.

Minimum On-Time and Off-Time

The shortest duration for the HS switch on-time (t_{ON_MIN}) is 110 ns (TYP). For the off-time (t_{OFF_MIN}) the minimum value is 80 ns (TYP). The duty cycle (or equivalently the V_{OUT}/V_{IN} ratio) range in CCM operation is limited by t_{ON_MIN} and t_{OFF_MIN} depending on the switching frequency. The minimum and maximum allowed duty cycles are given by Equations 2 and 3:

$$D_{MIN} = t_{ON\_MIN} \times f_{SW} \qquad (2)$$

And

$$D_{MAX} = 1 - t_{OFF\_MIN} \times f_{SW} \qquad (3)$$

Note that the duty cycle has a more limited range at higher frequencies. DMAX limits the lowest VIN voltage for a given VOUT.

For any given output voltage, the switching frequency is an important factor to maximize efficiency and input voltage range and minimize solution size. The highest input voltage can be calculated from:

$$V_{IN\_MAX} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN}} \qquad (4)$$

Due to losses in heavy load conditions there is a small increase in duty cycle and the actual VIN_MAX is higher than Equation 4 prediction.

The minimum VIN is estimated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{1 - f_{SW} \times t_{OFF\_MIN}} \qquad (5)$$

Compensation and Feed-Forward Capacitor (CFF)

The CE81D340MQ are internally compensated and are stable over the entire f_{SW} and V_{OUT} operating range. However, the phase margin can be low for some ranges of V_{OUT} when low ESR ceramic capacitors are used in the output. In such cases, it is recommended to use a feed-forward capacitor (C_{FF}) in parallel with the RFBT to improve the transient response as shown in Figure 4.

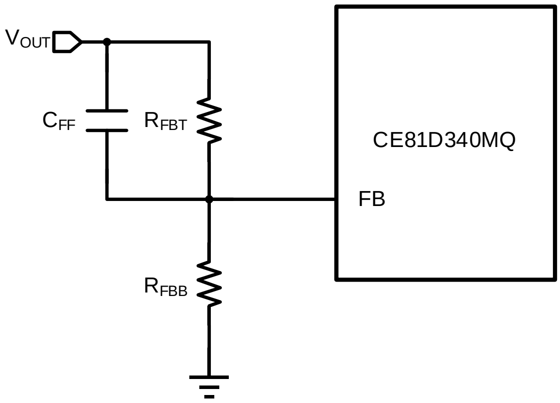


Figure 4.Improving Loop Compensation by Feed-Forward Capacitor

The C_{FF} in parallel with RFBT places an additional zero before the loop cross over frequency and boosts the phase margin. The zero will be located at:

$$f_{Z\_CFF} = \frac{1}{2\pi \times C_{FF} \times R_{FBT}} \qquad (6)$$

Refer to Table 1 for a list of suitable C_{OUT}, C_{FF} and R_{FBT} combinations. If for similar C_{OUT} values, other R_{FBT} values are used, adjust the C_{FF} such that ($C_{FF} \times R_{FBT}$) is unchanged. C_{FF} must also be modified if C_{OUT} is changed. For C_{OUT} capacitors with lower ESR, larger CFF values are needed. For example, with electrolytic capacitors (large ESR), the location of ESR zero, (Equation 7), is typically low enough for phase boost at crossover and CFF is not needed.

$$f_{Z\_ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR} \qquad (7)$$

Note that C_{FF} increases the feedback of the output ripple and the coupled noise to the FB node. A large C_{FF} value can deteriorate the V_{OUT} regulation. If significant derating for the C_{FF} value at cold operating temperatures is expected, it is better to use larger C_{OUT} capacitance rather than increasing the nominal C_{FF} value.

Over-Current Protection (OCP) and Short-Circuit Protection (SCP) Protection

Cycle-by-cycle current limit for both peak and valley currents (upper and lower switches peak currents) are included in the CE81D340MQ. If the OCP or SCP persists, it will enter hiccup mode to avoid thermal shutdown.

The HS switch over-current protection is natural in peak current mode control. In each cycle the HS current sensing starts a short time (blanking time) after it is turned on. The slope compensation ramp is deducted from the EA (Error Amplifier) output to avoid sub harmonic oscillations and the result is compared to the HS current to determine the HS turn-off time (on-time). Before comparison, the EA output is clamped to a fixed maximum threshold (I_{HS_LIMIT}) to limit the current. So, the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

When the LS switch turns on the inductor current starts falling. The LS current is sensed while it is on and the switch will not turn off at the end of cycle if this current is still higher than its limit (I_{LS_LIMIT}) and keeps conducting until the current falls below I_{LS_LIMIT}. During OCP or SCP, the LS current limit is not effective until the HS current limit is triggered.

A short dead time is considered after the LS switch is turned off, in which both switches are kept off and then a new cycle starts by turning the HS switch on.

If the LS switch over-current detection continues for 128 successive cycles, hiccup current protection will be started in which the regulator remains off for 30ms (TYP) before restarting the converter. If OCP or SCP is still detected after this restart, a new hiccup cycle will be repeated. Hiccup mode is considered to protect the device from overheating and damage in severe over-current conditions.

Under-voltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When input voltage increases up to the upper threshold of UVLO, it begins to switch.

Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 175 °C), the device is shut off. When the temperature falls to about 155 °C or below, the convertor begins to switch.

Standby Operation

When the CE81D340MQ is operating in either normal CCM or PFM, they may be placed in standby by pulling the EN pin to low.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameters	Min	Max	Unit
V_I	VIN Voltage Range	-0.3	42	V
	EN/SYNC Voltage Range	-5.5	V_{IN}+0.3	V
	VCC Voltage Range	-0.3	5.5	
	VFB Voltage Range	-0.3	4.5	V
	BOOT(VS SW) Voltage Range	-0.3	5.5	V
	SW Voltage Range	-0.3	V_{IN}+0.3	V
	SW (10ns transient)	-5	42	V
V_{ESD}	Human Body Model (JEDEC JS-001)		±2000	V
	Charged Device Model (JESD22-C101)		±1000	V
T_J	Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-65	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameters	Min	Typ	Max	Unit
V_{IN}	Supply Input Voltage Range (VIN)	4.5		36	V
V_{OUT}	Output Voltage Range	0.8		24	V
I_{OUT}	Output current Range			3	A
T_A	Ambient Temperature	-40		125	°C

Thermal Properties

Symbol	Parameters	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	52	°C/W

Electrical Characteristics

V_{IN} = 12 V, T_J = -40 °C to 125 °C, typical values are at T_J = +25 °C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Current						
I_{IN}	Operating–non-switching Supply Current into VIN	V_{IN}=12 V, EN = 5 V,V_{FB} = 0.9 V		64		μA
I_{IN_OFF}	Shutdown supply current into VIN	V_{IN}=12 V,EN = 0 V, T_J =-40 °C to 125 °C		0.6	1.8	μA
Logic Threshold						
V_{EN_H}	EN High-level Input Voltage		1.35	1.50	1.65	V
V_{EN_L}	EN Low-level Input Voltage			1.07		V
V_{EN_HYS}	Enable Hysteresis			430		mV
I_{EN}	Input Leakage Current at EN Pin	V_{IN}=4.5 to 36V,V_{EN} = 2V, T_J =-40 °C to 125 °C		10	500	nA
		V_{IN}=V_{EN}=36 V			1	μA
V_{FB} Voltage						
V_{FBTH}	V_{FB} Threshold Voltage	V_{IN}=6 to 36 V,T_J =25 °C	0.782	0.804	0.824	mV
	V_{FB} Threshold Voltage	V_{IN}=6 to 36 V, T_J =-40 °C to 125 °C	0.780	0.804	0.826	mV
I_{FB}	V_{FB} Input Current	V_{FB} = 0.8 V		10		nA
Internal LDO						
V_{CC}	Internal LDO Output Voltage	V_{IN}=6 to 36 V, T_J =-40 °C to 125 °C	4.6	5.0	5.3	V
MOSFET						
$R_{DS(ON)\_H}$	High-side Switch Resistance	V_{IN}=12 V,I_{VIN-SW} = 0.5 A		115		mΩ
$R_{DS(ON)\_L}$	Low-side Switch Resistance	V_{IN}=12 V,I_{SW} = 0.5 A		90		mΩ
Current Limit						
I_{HS_LIMIT}	Peak Inductor Current Limit	T_J =25 °C	5.0	5.9	6.8	A
I_{LS_LIMIT}	Valley Inductor Current Limit	T_J =25 °C	2.2	2.9	3.5	A
Thermal Shutdown						
T_{SDN}	Thermal Shutdown Threshold	Shutdown temperature		175		°C
T_{SDN_HYS}		Hysteresis		20		°C
ON/OFF-Time Timer Control						
$t_{ON(MIN)}$	Minimum on Time			110		ns
$t_{OFF(MIN)}$	Minimum off Time			80		ns
Frequency						
F_{SW}	Switching Frequency	CCM mode	310	390	470	KHz
Soft Start						
T_{SS}	Soft Start Time	The time of internal reference to increase from 0V to 0.8 V.		1.5		ms

Electrical Characteristics(Continued)

V_{IN} = 12 V, T_J = -40 °C to 125 °C, typical values are at T_J = +25 °C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Hiccup Mode						
N_{OC}[(1)]	Number of Cycles that LS Current Limit is Tripped to Enter Hiccup Mode			128		Cycles
t_{OC}	Hiccup Retry Delay Time			30		ms
UVLO						
V_{UVLO}	UVLO Threshold	Wake up V_{IN} voltage	4.1	4.3	4.5	V
		Shutdown V_{IN} voltage		4.01		
		Hysteresis V_{IN} voltage		0.29		
SYNC (EN/SYNC Pin)						
f_{SYNC}	SYNC Frequency Range		200		2200	kHZ
V_{SYNC}	Amplitude of SYNC Clock AC Signal (Measured at SYNC Pin)		2.8		5.5	V
t_{SYNC_MIN}	Minimum SYNC Clock On/Off Time			100		ns

Note1: Not production tested, design assurance.

Application and Implementation

Note

Information in the following applications sections is not part of the CTK component specification. CTK does not warrant its accuracy or completeness and Customers should be responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

CE81D340MQ is typical step-down DC-DC converter. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the CE81D340MQ.

Typical Application

The application schematic below was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

The Figure 5 shows CE81D340MQ converter schematics.

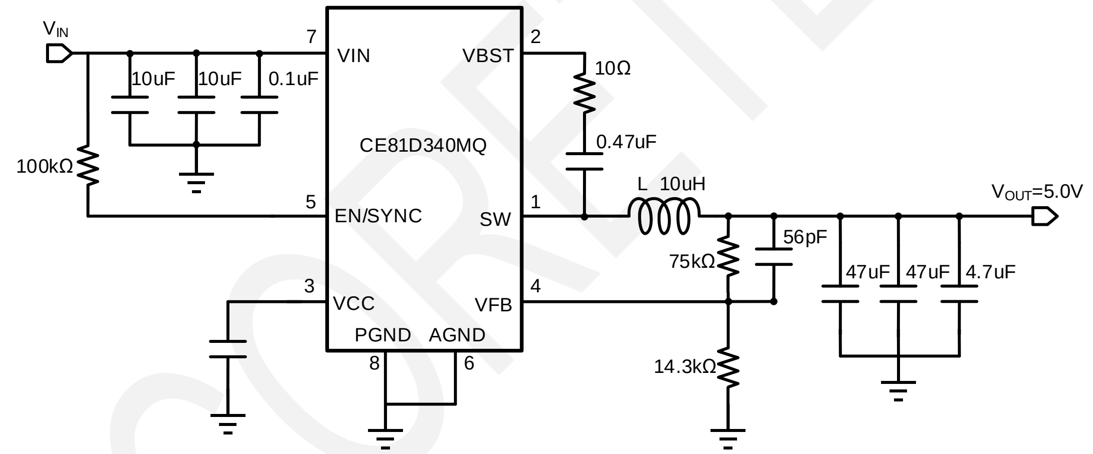


Figure 5.Basic Application Schematic

The external components are designed based on the application requirements and device stability. Some suitable output filters (L and C_{OUT}) along with C_{FF} and R_{FBT} values are provided in Table1 to simplify component selection. Consider the following notes when using this table.

1. Choose the inductance for VIN = 36 V.

2. C_{OUT} values in the table are actual derated values. Use higher nominal values for ceramic capacitors.

3. Use R_{FBT} = 0 Ω to set V_{OUT} = 0.804 V. Use R_{FBB} = 14.3 kΩ for any other VOUT setting.

4. If any other R_{FBT} value is designed, resize C_{FF} to keep ($C_{FF} \times R_{FBT}$) unchanged.

5. If the selected output capacitance has high ESR, the C_{FF} is not necessary for extra phase boost.

Table 1. Some Typical L, C_{OUT} and C_{FF} Values for Stable Operation

V_{OUT} (V)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	L (μH)	C_{OUT} (μF)	C_{FF} (pF)	f_{SW} (kHz)
3.3	44.2	14.3	6.8	150	75	390
5	75	14.3	10	100	56	390
12	200	14.3	15	68	-	390
24	412	14.3	15	47	-	390

Design Requirements

This table below shows the design parameters for this application.

Parameter	Example Value
Input voltage range	12 V (TYP),variation range is from 8 to 28 V
Output voltage	5 V
Maximum Output Current	3 A
Transient response, 1.5 A load step	ΔV_{OUT} = ±2.5 %
Input ripple voltage	400 mV
Output ripple voltage	50 mV
Operating frequency	390 kHz

Detailed Design Procedure

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. CTK recommends using 1% tolerance or better divider resistors. Start by using Equation 8 to calculate VOUT.For example, by choosing RFBB = 14.3 kΩ, the RFBT value for 5 V output will be calculated as 75 kΩ.

If customers want to improve efficiency at very light loads,we recommend using larger value resistors. High value of resistor will be more susceptible to noise and voltage errors from the V_{FB} input current will be more noticeable.

$$V_{OUT} = 0.804 \times (1 + \frac{R_{FBT}}{R_{FBB}}) \qquad (8)$$

Output Capacitor Selection

The main factors for designing C_{OUT} are output voltage ripple, control loop stability and the magnitude of output voltage overshoot/undershoot after a load transients.

The output voltage ripple has two main components. One is due to the ac current (ΔI_L) going through the capacitor ESR:

$$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR = K_{IND} \times I_{OUT} \times ESR \qquad (9)$$

and the other one is caused by the charge and discharge of capacitor by the ac current (ΔI_L):

$$\Delta V_{OUT\_C} = \frac{\Delta I_L}{(8 \times f_{SW} \times C_{OUT})} = \frac{K_{IND} \times I_{OUT}}{(8 \times f_{SW} \times C_{OUT})} \qquad (10)$$

These AC components are not in phase and the total peak-to-peak ripple is less than ΔV_{OUT_ESR} + ΔV_{OUT_C}.

In many applications, tight regulation in response to large and fast load transients is required. This can be a more severe condition on designing C_{OUT} value. Typically the control loop recovers the output voltage after four or five cycles and C_{OUT} should be large enough to provide the difference between current received from inductor and the current delivered to the load during this period. The minimum capacitance needed to limit the undershoot to V_{US} when the load steps up from I_{OL} to I_{OH} is given in Equation 11. Similarly, when the load steps from I_{OH} down to I_{OL}, C_{OUT} should be large enough to absorb the extra energy coming from the inductor without a large voltage overshoot (V_{OS}) as calculated in Equation 12:

$$C_{OUT} > \frac{4 \times (I_{OH} - I_{OL})}{f_{SW} \times V_{US}} \qquad (11)$$

$$C_{OUT} > \frac{(I_{OH}^2 - I_{OL}^2)}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \times L \qquad (12)$$

In this example, maximum acceptable ripple is 50 mV. Assuming ΔV_{OUT_ESR} = ΔV_{OUT_C} = 50 mV and K_{IND} = 0.4. Equation 9 results in ESR < 41.7 mΩ and Equation 10 leads to C_{OUT} > 7.5 μF. If the overshoot/undershoot transient requirement is 5% then V_{US} = V_{OS} = 5% × VOUT= 250 mV. Equations 11 and 12, I_{OH} = 2.5 A, I_{OL} = 0.2 A, lead to C_{OUT} > 94 μF and C_{OUT} > 24 μF respectively. Now considering all conditions and including voltage derating of the ceramic capacitors, C_{OUT} is composed of a 47 μF/16V ceramic capacitor parallel with a 100 μF/10 V capacitor with 5 mΩ ESR.

Input Capacitor Selection

High frequency decoupling on the input supply pins is necessary for the device. A bulk capacitor may also be needed in some applications. Typically, 10 μF to 22 μF high quality ceramic capacitor (X5R, X7R or better) with voltage rating twice the maximum input voltage is recommended for decoupling capacitor. If the source is away from the device (> 5cm) some bulk capacitance is also needed to damp the voltage spikes caused by the wiring or PCB trace parasitic inductances. In this example, 2×10 μF/50V/X7R capacitors and a 0.1 μF ceramic capacitor placed right beside the device VIN and GND pins for very high-frequency filtering are used.

Inductor Selection

Three main inductor parameters that need to be designed are inductance, saturation current and rated current. The DCR is also an important factor for efficiency. Physical dimensions, form factor and shielded or non-shielded structure are other important factors that are selected based on the application. The inductance is designed by selecting the peak-to-peak current ripple (ΔI_L) that is given by Equation 13. ΔI_L is increase at higher input voltages, so V_{IN_MAX} is used in the equation. The minimum required inductance (L_{MIN}) is calculated from Equation 14. K_{IND} represents the ratio of inductor ripple current to the maximum output current ($K_{IND} = \Delta I_L / I_{OUT\_MAX}$). It is typically chosen between 20% to 40%.

$$\Delta I_L = \frac{V_{OUT}}{V_{IN\_MAX}} \times \frac{V_{IN\_MAX} - V_{OUT}}{L \times f_{SW}} \quad (13)$$

$$L_{MIN} = \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \times \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \quad (14)$$

During a short or over current, either RMS or peak inductor current can increase significantly. The inductor rated RMS and saturation current ratings should be higher than those peaks respectively. It is generally desired to choose an smaller inductance value to have faster transient response, smaller size, and lower DCR. However, reducing the inductance increases the current ripple that may result in over current detection and triggering OCP before reaching full load current. Moreover, higher current ripple increases core, conduction, and capacitor losses. Output voltage ripple will also be higher with the same output capacitance. In general, choosing a too small inductance is not recommended for peak current mode control. On the other hand, too large inductance is also not recommended, because the reduced current ripple degrades the comparator signal to noise ratio.

Selecting K_{IND} = 0.4 results in L_{MIN} = 8.78μH. A 10μH ferrite inductor with 5A RMS rating and 7.6 A saturation current is selected as the closest standard value

Bootstrap Capacitor Selection

The bootstrap capacitor powers the floating power MOSFET driver. It is recommended to use 0.47μF/16V/X5R ceramic capacitor.

The value of BST resistor generally is recommended to be in the range from 0 to 10 Ω. BST resistor determines the turning on speed of the high side MOSFET. For the design where the critical path layout could not be optimized and follow the recommended layout, the 10 Ω BST resistor is recommended to be used to in series with the Bootstrap capacitor.

Feed-Forward Capacitor Selection

Even though the CE81D340MQ are internally compensated, with low ESR ceramic capacitors, the phase margin can be low depending on the V_{OUT} and f_{SW} values. By adding an external feed-forward capacitor (C_{FF}) in parallel with the R_{FBT}, the phase margin can be improved (phase boost around crossover frequency). Without C_{FF}, and if ESR is very small, the crossover frequency (f_X) can be estimated from Equation 15, in which C_{OUT} is the actual derated value:.

$$f_X = \frac{8.32}{V_{OUT} \times C_{OUT}} \quad (15)$$

Then C_{FF} value can be estimated from:

$$C_{FF} = \frac{1}{4\pi \times f_X \times R_{FBT}} \quad (16)$$

For slightly larger ESR values, choose a C_{FF} value that is less than Equation 16 estimate. For larger ESR values, C_{FF} is not needed. Table 1 gives a quick starting point. In this example, a 56 pF/50V/COG is selected for C_{FF}.

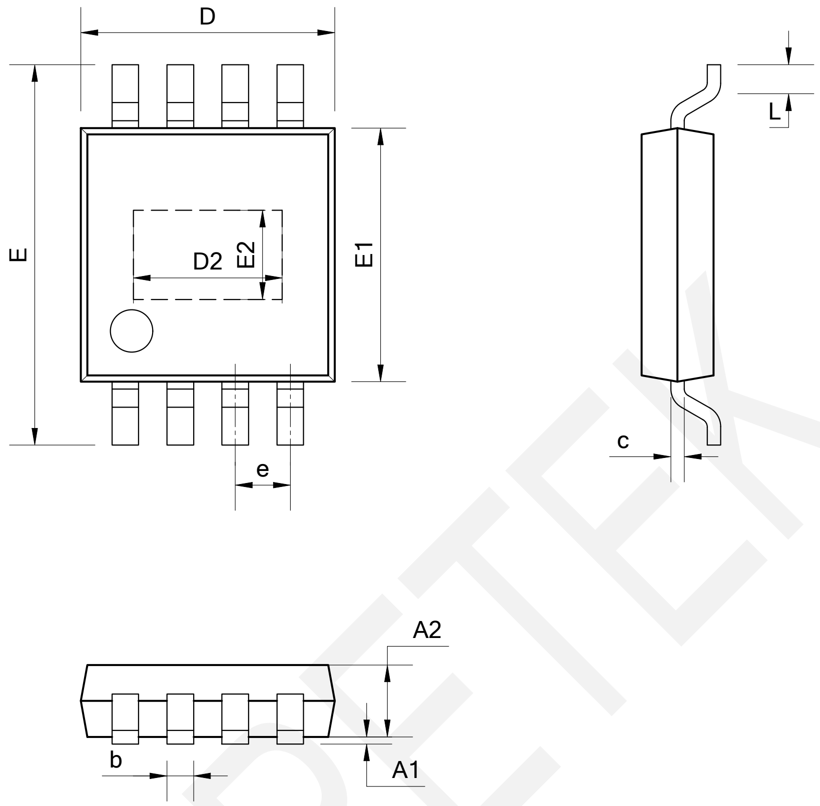
VCC Decoupling Capacitor Selection (LDO Output)

Use a 2.2 μF/16V/X7R capacitor for decoupling VCC to assure stability of the device. It must be placed with minimum distance between VCC and GND pins.

Application Curves

Package Dimension

ESOP8



Dimensions Table (Units: mm)

SYMBOL	MIN	NOM	MAX
A1	0.00	-	0.15
A2	1.35	1.40	1.50
b	0.38	-	0.47
c	0.17	-	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
D2	3.02	3.17	3.32
E1	3.80	3.90	4.00
E2	2.13	2.28	2.43
e	1.17	1.27	1.37
L	0.45	0.60	0.80

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2025.12.27	Preliminary Version	LiuCong	Xie Lin Han	Xie Lin Han