

CE81D31 - 4.5V to 17V Input, 3A Synchronous Step-Down Regulator

General Description

The CE81D31 is a highly integrated, wide input voltage, 3 A output synchronous buck convertor.

The device is optimized to operate with minimum external component counts and also optimized to achieve low standby current.

This convertor adopts adaptive constant-on-time (ACOT) structure, and provides a fast transient response. It also supports both low-equivalent series resistance (ESR) output capacitors and ultra-low ESR ceramic capacitors with no external compensation components.

During light load operation, CE81D31 operates in pulse frequency modulation (PFM) mode, which maintains high efficiency.

Features

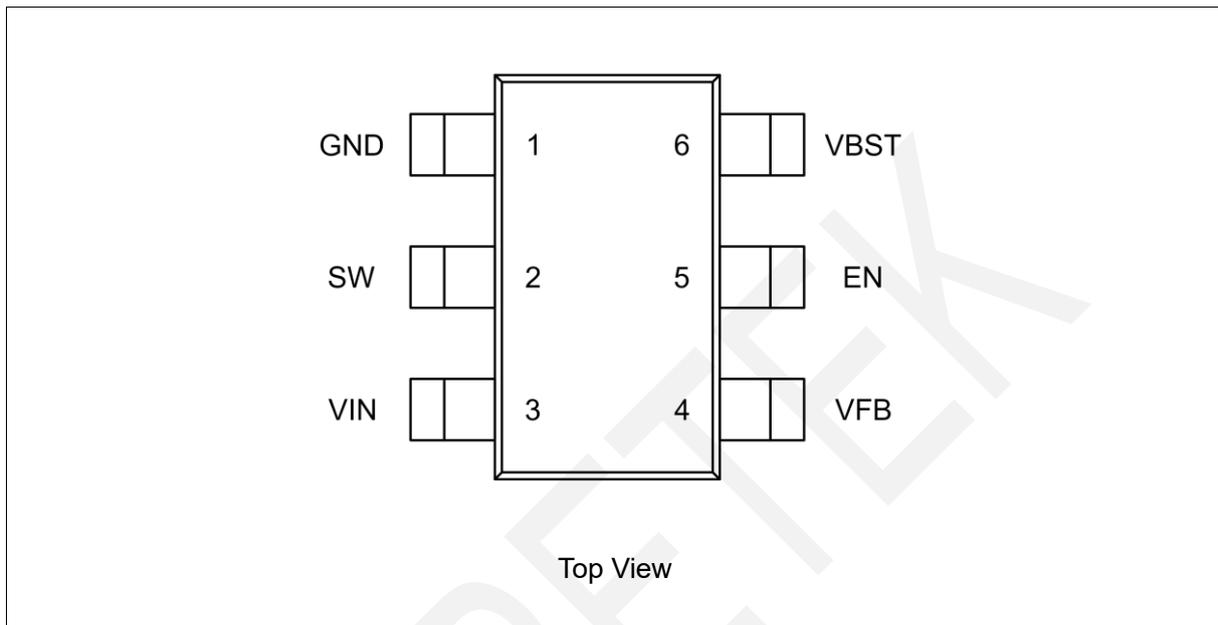
- 3 A Converters Integrated 90 mΩ and 50 mΩ FET
- ACOT Mode Control with Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- PFM Mode during Light Load Operation
- 580 kHz Switching Frequency
- Low Shutdown Current Less than 5 μA
- Start-up from Pre-Biased Output Voltage
- Cycle-by-Cycle Over-current Limit
- Hiccup-mode Over-current Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.0 ms
- ESD protection
 - HBM ±3KV PASS
 - CDM ±1KV PASS
- Part No. and Package

Part No.	Package	Packing Option	MSL
CE81D31	SOT23-6 (2.9 mm × 2.8 mm)	Tape and Reel, 3K/Reel	3

Application

- Digital TV Power Supply and Surveillance
- Disc Players
- Networking Home Terminal
- Digital Set Top Box

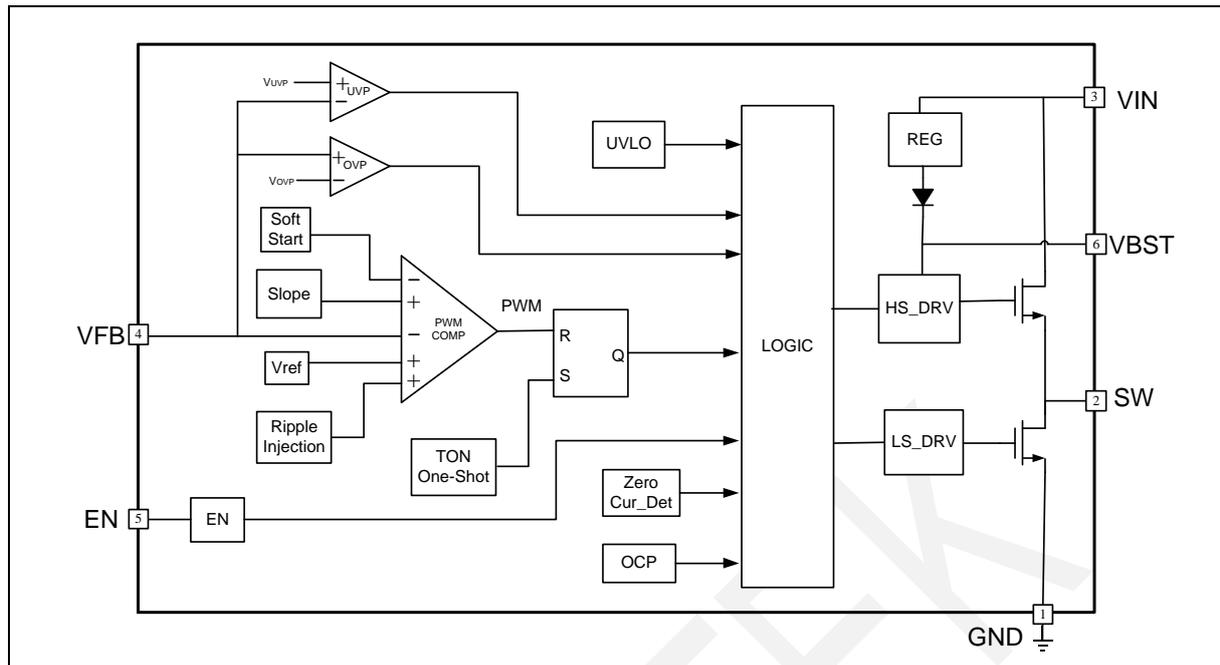
Pin Configuration



Pin Function

Pin Name	Pin No.	I/O	Description
GND	1		Ground pin of controller circuit, as well as source terminal of low-side power NFET. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between low-side NFET and high-side NFET.
VIN	3	I	Input voltage supply pin, also the drain terminal of high-side power NFET.
VFB	4	I	Output voltage feedback pin. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable pin. Must be pulled up to enable the device.
VBST	6	O	Power supply of high-side NFET control circuit. Connect 0.1 μ F capacitor between VBST and SW pins.

Block Diagram



Functional Description

Overview

The CE81D31 is highly integrated, 3 A synchronous buck converter. It employs adaptive constant on time (ACOT) mode, and supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of this device can reduce the output capacitance.

Adaptive On-Time Control and PWM Operation

The main control mode of CE81D31 is pulse width modulation (PWM) with ACOT structure. This control mode control can achieve pseudo-fixed frequency and stable operation with both low-ESR and ceramic output capacitors.

The high-side MOSFET is turned on at the beginning of each cycle. When one shot timer expires, the high-side power FET is turned off. This one shot duration is set proportional to input voltage, V_{IN} , and inversely proportional to the output voltage, V_O , to achieve pseudo-fixed frequency over the input voltage range, hence it is called adaptive constant on-time control. The one-shot timer is reset and the high-side power FET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is generated to emulate output ripple, eliminating the need for ESR of output capacitor.

Pulse Frequency modulation

The CE81D31 is designed with pulse frequency modulation mode to achieve high efficiency during light load condition. As the output current decreases from heavy load condition, the inductor current also decreases and eventually comes to zero, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side power FET is turned off when the zero inductor current is detected. As the load current further decreases the converter enters into discontinuous conduction mode. The on-time is almost the same as it was in the continuous conduction mode so that it takes longer time to

discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps efficiency high in light load condition. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{sw}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

In PFM mode, each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the threshold voltage. As the output current decreases, the sleep time between switching pulses increases.

Soft Start and Pre-Biased Soft Start

The CE81D31 is designed with an internal 1ms soft-start. When the VIN is plugged in and the EN pin becomes high, the reference voltage of PWM comparator begins to rise from zero.

If the output capacitor is pre-biased at start-up, the device begins to switch and start ramping up only after the internal reference voltage becomes greater than the feedback voltage VFB. This scheme ensures that the converters ramp up smoothly into regulation point.

Current Protection

The over-current limit (OCL) is implemented by using cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET drain to source voltage during its on-state. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-state of high-side FET, the switch current increases at a linear rate determined by V_{IN} , V_{OUT} , and the inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT} . If the monitored current is above the OCL level, the converter keeps low-side FET on and prevents the creation of a new set pulse, even the voltage feedback loop requires one, until the current level decreases to OCL level or lower. In next switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the load current is higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time and re-start after the hiccup time (typically 12 ms). When the over current condition is removed, the output voltage returns to the regulated value.

Under-voltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When input voltage increases up to the upper threshold of UVLO, it begins to switch.

Thermal Shutdown

The device monitors the temperature of itself. If temperature exceeds the threshold value (typically 170 °C), the device is shut off. When the temperature falls to about 140 °C or below, the converter begins to switch.

Standby Operation

When the CE81D31 is operating in either normal CCM or PFM, they may be placed in standby by pulling the EN pin to low.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)

Parameters		Min	Max	Unit
Input Voltage	V _{IN,EN}	-0.3	19	V
	V _{BST}	-0.3	24	V
	V _{BST} (10ns transient)	-0.3	25	V
	V _{BST} (VS SW)	-0.3	6.5	V
	V _{FB}	-0.3	6.5	V
	SW	-2	19	V
	SW (10ns transient)	-3.5	20	V
V _{ESD}	Human Body Model (JEDEC JS-001)		±3000	V
	Charged Device Model (JESD22-C101)		±1000	V
R _{θJA}	Junction-to-ambient thermal resistance		93	°C/W
R _{θJC}	Junction-to-case thermal resistance		49	°C/W
T _J	Junction Temperature	-40	+150	°C
T _{STG}	Storage Temperature	-65	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameters	MIN	MAX	Unit
V _{IN}	Supply Input Voltage Range	4.5	17	V
V _I	V _{BST}	-0.1	22	
	V _{BST} (10ns transient)	-0.1	25	
	V _{BST} (VS SW)	-0.1	6	
	EN	-0.1	17	
	V _{FB}	-0.1	5.5	
	SW	-1.8	18	
	SW (10ns transient)	-3.5	20	
T _J	Operating Junction Temperature	-40	125	°C
T _A	Ambient Temperature	-40	85	°C

Electrical Characteristics

$V_{IN} = 12\text{ V}$, $T_A = -40^\circ\text{C}$ to 85°C , (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Current						
I_{VIN}	Operating–non-switching Supply Current	V_{IN} current, $EN = 5\text{ V}, V_{FB} = 0.8\text{ V}$		420	520	μA
I_{VNSDN}	Shutdown supply current	V_{IN} current, $EN = 0\text{ V}$		1.6	5	
Logic Threshold						
V_{ENH}	EN High-level Input Voltage	To make sure the device is enabled, V_{ENH} should be bigger than 1.6 V	1.1	1.3	1.6	V
V_{ENL}	EN Low-level Input Voltage	To make sure the device is disabled, V_{ENL} should be smaller than 0.8 V	0.8	1.2	1.4	
R_{EN}	EN Pin Resistance to GND	$V_{EN} = 12\text{ V}$	200	320	600	$\text{k}\Omega$
V_{FB} Voltage and Discharge Resistance						
V_{FBTH}	V_{FB} Threshold Voltage	$V_O = 1.05\text{ V}$, $I_O = 10\text{ mA}$, PFM operation		775		mV
	V_{FB} Threshold Voltage	$V_O = 1.05\text{ V}$, Continuous mode operation	741	760	779	mV
I_{VFB}	V_{FB} Input Current	$V_{FB} = 0.8\text{ V}$			0.1	μA
MOSFET						
$R_{DS(ON)H}$	High-side Switch Resistance	$T_A = 25^\circ\text{C}$, $V_{BST} - SW = 5\text{ V}$		90		$\text{m}\Omega$
$R_{DS(ON)L}$	Low-side Switch Resistance	$T_A = 25^\circ\text{C}$		50		$\text{m}\Omega$
Current Limit						
I_{OCL}	Current Limit	DC current, $V_{OUT} = 1.05\text{ V}$, $L_1 = 1.5\text{ }\mu\text{H}$	3.5	4.8	5.5	A
Thermal Shutdown						
T_{SDN}	Thermal Shutdown Threshold ⁽¹⁾	Shutdown temperature		170		$^\circ\text{C}$
		Hysteresis		30		
ON-Time Timer Control						
$t_{OFF(MIN)}$	Minimum off Time	$V_{FB} = 0.5\text{ V}$		310		ns
Soft Start						
t_{SS}	Soft Start Time	Internal soft-start time		1.0		ms
Frequency						
F_{SW}	Switching Frequency	$V_{IN} = 12\text{ V}$, $V_O = 1.05\text{ V}$, CCM mode	522	580	638	KHz

Note1: Not production tested, design assurance.

Electrical Characteristics(Continued)

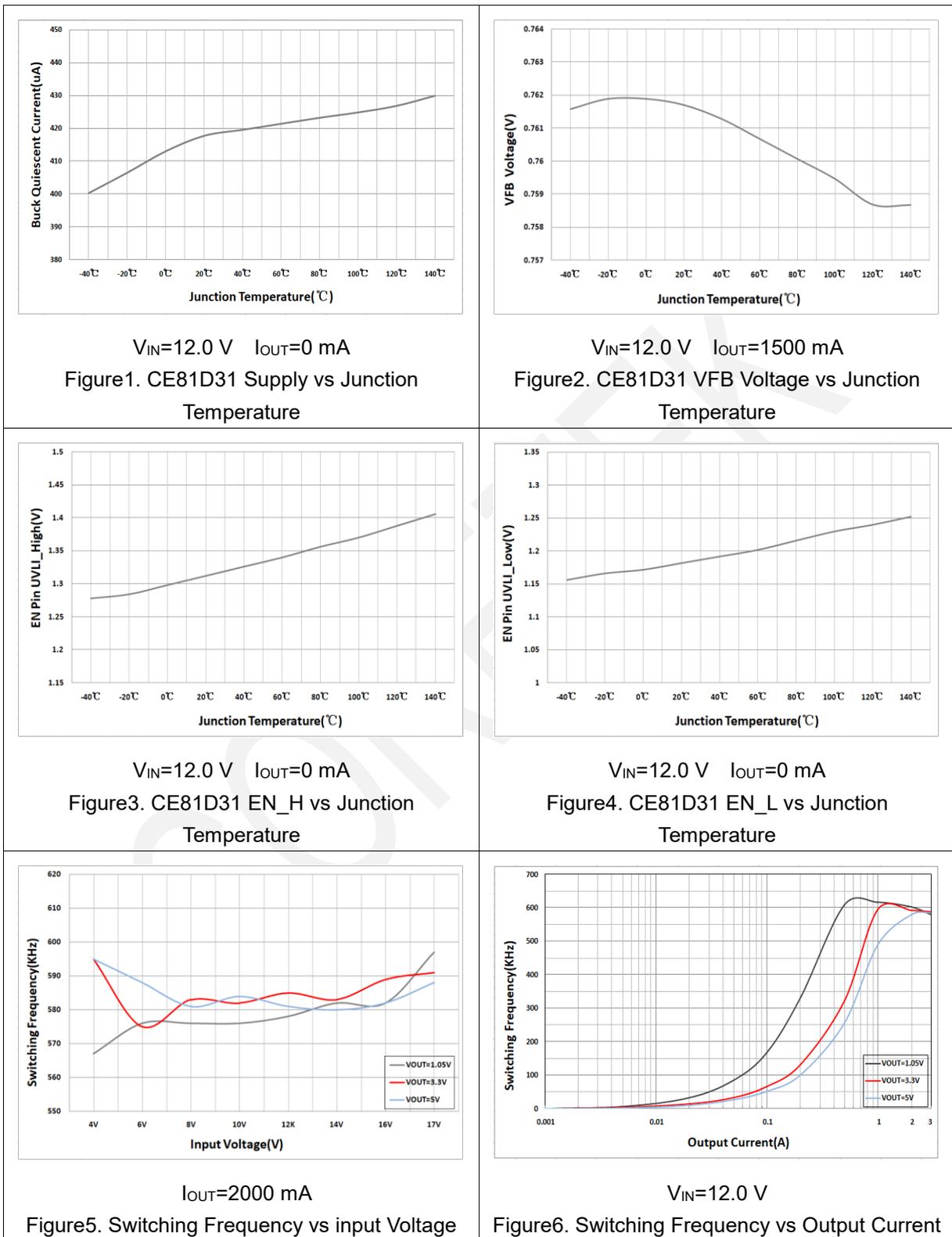
$V_{IN} = 12\text{ V}$, $T_A = -40^{\circ}\text{C}$ to 85°C , (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Output Under-voltage and Over-voltage Protection						
V_{UVP}	Output UVP Threshold	Hiccup detect ($H > L$)		64		%
t_{HICCUP_WAIT}	Hiccup on Time			1.4		ms
t_{HICCUP_RE}	Hiccup Time Before Restart			12		ms
UVLO						
V_{UVLO}	UVLO Threshold	Wake up V_{IN} voltage	3.8	4.1	4.3	V
		Shutdown V_{IN} voltage	3.3	3.6	3.8	
		Hysteresis V_{IN} voltage		0.5		

Note(1). Not production tested, design assurance.

Typical Characteristics

$V_{IN} = 12\text{ V}$ (unless otherwise noted)



Typical Characteristics(Continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

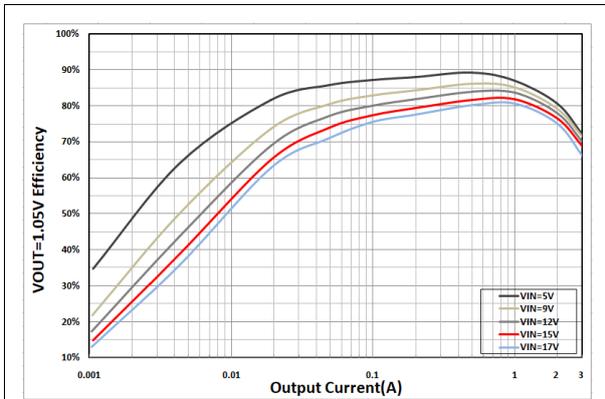


Figure7. $V_{OUT}=1.05\text{ V}$ Efficiency
 $L=2.2\text{ }\mu\text{H}$

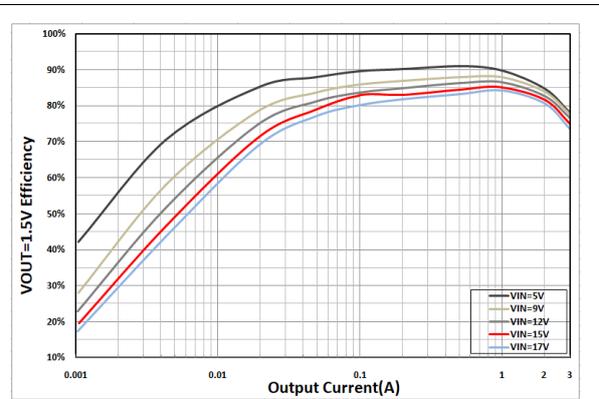


Figure8. $V_{OUT}=1.5\text{ V}$ Efficiency
 $L=2.2\text{ }\mu\text{H}$

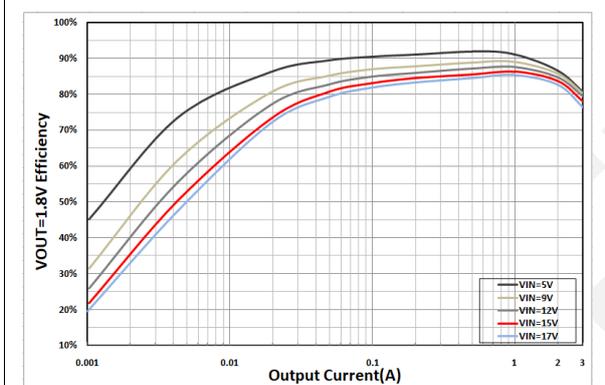


Figure9. $V_{OUT}=1.8\text{ V}$ Efficiency
 $L=2.2\text{ }\mu\text{H}$

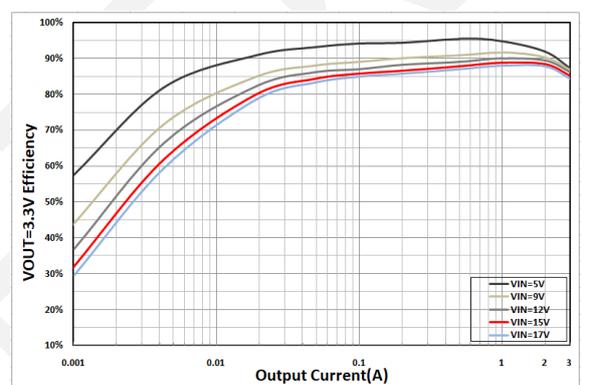


Figure10. $V_{OUT}=3.3\text{ V}$ Efficiency
 $L=2.2\text{ }\mu\text{H}$

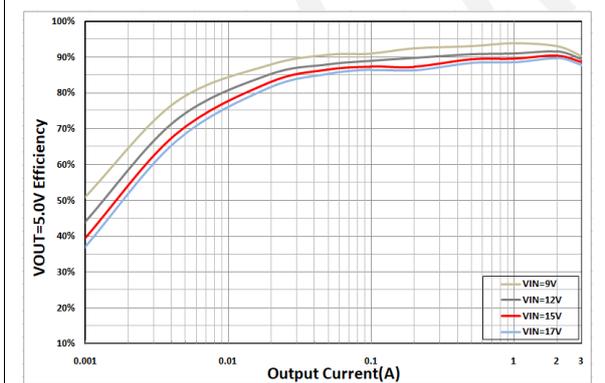


Figure11. $V_{OUT}=5.0\text{ V}$ Efficiency
 $L=2.2\text{ }\mu\text{H}$

Application and Implementation

Note

CTK don't warrant its accuracy or completeness and Information in the following applications sections is not part of the CTK component specification. Customers should be responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

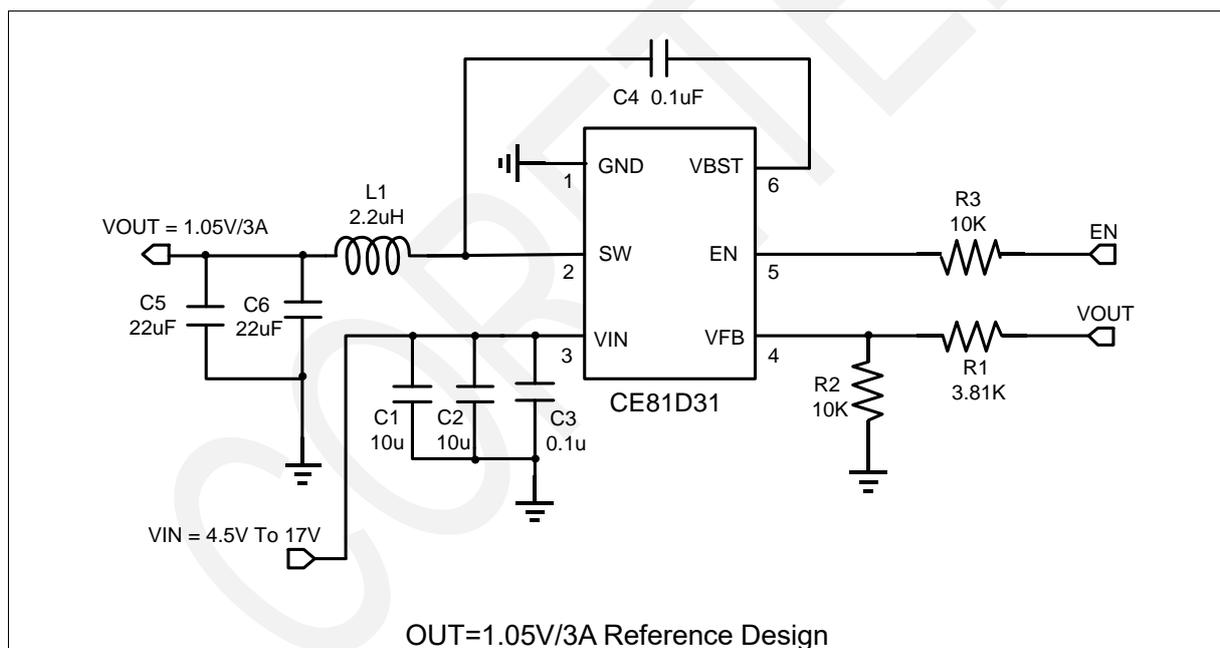
Application Information

CE81D31 is typical step-down DC-DC converter. It's typically used to convert a higher DC voltage to a lower DC voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the CE81D31.

Typical Application

The application schematic below was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

The figure shows CE81D31 4.5 V to 17 V input, 1.05 V output converter schematics.



Design Requirements

This table below shows the design parameters for this application.

Parameter	Example Value
Input voltage range	4.5 to 17V
Output voltage	1.05V
Transient response, 1.5A load step	$\Delta V_{OUT} = \pm 2.5\%$
Input ripple voltage	400mV
Output ripple voltage	30mV
Output current rating	3A
Operating frequency	580KHz

Detailed Design Procedure

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. CTK recommends using 1% tolerance or better divider resistors. Start by using [Equation 2](#) to calculate V_{OUT}.

If customers want to improve efficiency at very light loads, we recommend using larger value resistors. High value of resistor will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.76 \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

The overall loop gain is set by the output set-point resistor divider network and the internal gain of the device at low frequencies. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a -40dB per decade rate and the phase drops rapidly. The inductor and capacitor for the output filter should be selected so that the double pole of [Equation 3](#) is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, use the values recommended in [Table 1](#).

Output Voltage (V)	R1(kΩ)	R2 (kΩ)	L1 (μH)			C5 + C6 (μF)
			Min	Typ	Max	
1.0	3.15	10.0	1.5	2.2	4.7	20 to 68
1.05	3.81	10.0	1.5	2.2	4.7	20 to 68
1.2	5.79	10.0	1.5	2.2	4.7	20 to 68
1.5	9.74	10.0	1.5	2.2	4.7	20 to 68
1.8	13.7	10.0	1.5	2.2	4.7	20 to 68
2.5	22.9	10.0	2.2	2.2	4.7	20 to 68
3.3	33.4	10.0	2.2	2.2	4.7	20 to 68
5.0	55.79	10.0	3.3	3.3	4.7	20 to 68
6.5	75.5	10.0	3.3	3.3	4.7	20 to 68

Table 1. Recommended Component Values

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using [Equation 4](#), [Equation 5](#), and [Equation 6](#). The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{p-p} = \frac{V_{OUT}}{V_{IN}(MAX)} \times \frac{V_{IN}(MAX) - V_{OUT}}{L_O \times f_{sw}} \quad (4)$$

$$I_{peak} = I_O + \frac{I_{p-p}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 3.5 A and the calculated RMS current is 3.01 A.

The inductor should be used with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The CE81D31 is intended for use with ceramic or other low ESR capacitors. We recommend using values range from 20 uF to 68 uF. Equation 7 determines the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{sw}} \quad (7)$$

Two 22 μF output capacitors are used for this design. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 3 A.

Input Capacitor Selection

The CE81D31 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. We recommend a ceramic capacitor over 10 uF for the decoupling capacitor. An additional 0.1uF capacitor (C3) from VIN pin to GND is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1 uF ceramic capacitor must be connected between the VBST to SW pin for proper operation. We recommend using a ceramic capacitor.

Power Supply Recommendations

CE81D31 is designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is $V_{OUT}/0.75$.

Application Curves

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

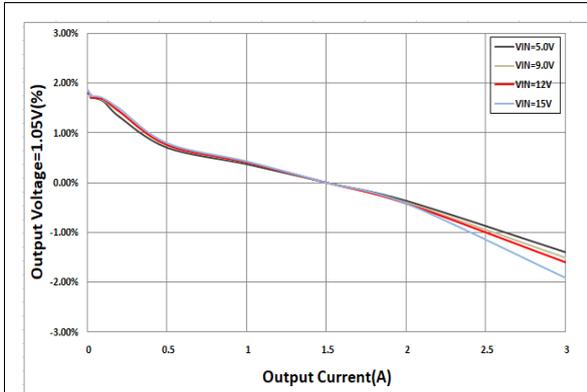


Figure12. CE81D31 Load Regulation,
 $V_{OUT}=1.05\text{ V}$

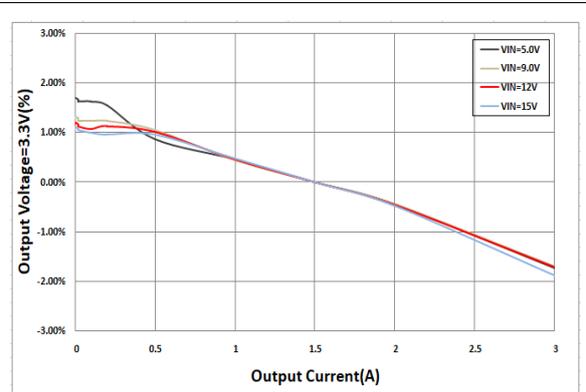


Figure13. CE81D31 Load Regulation,
 $V_{OUT}=3.3\text{ V}$

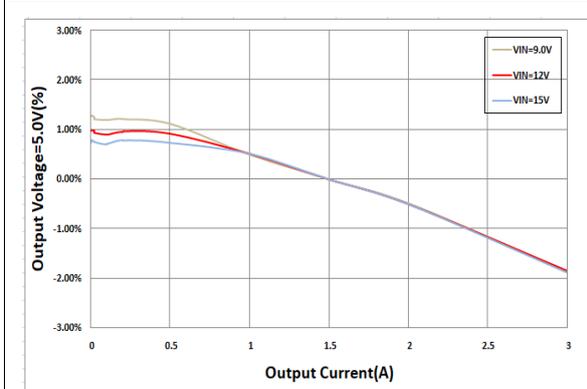


Figure14. CE81D31 Load Regulation,
 $V_{OUT}=5.0\text{ V}$

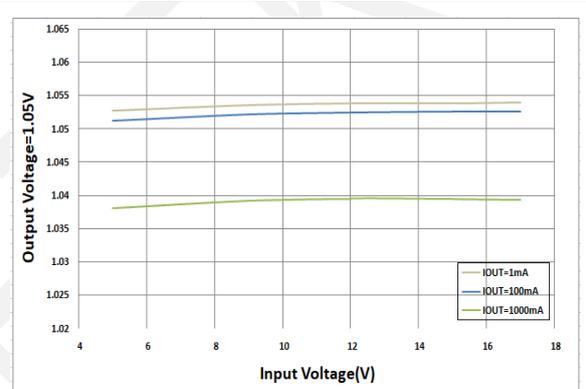


Figure15. CE81D31 Line Regulation,
 $V_{OUT}=1.05\text{ V}$

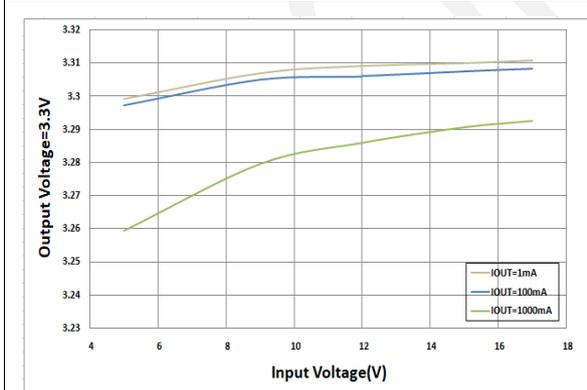


Figure16. CE81D31 Line Regulation,
 $V_{OUT}=3.3\text{ V}$

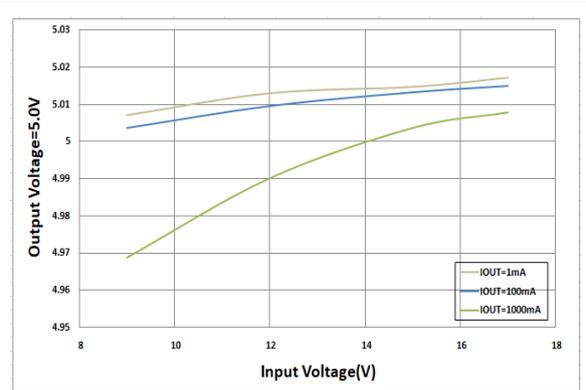


Figure17. CE81D31 Line Regulation,
 $V_{OUT}=5.0\text{ V}$

Application Curves(Continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

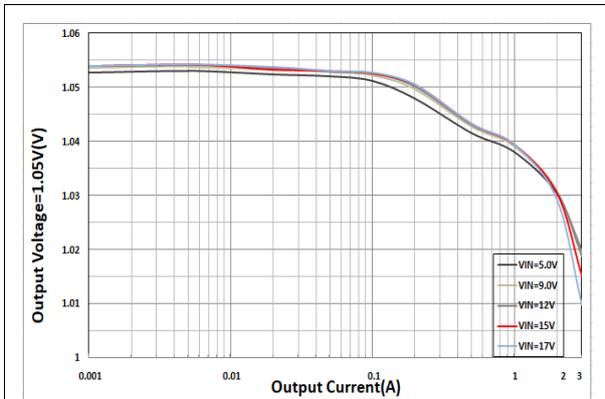


Figure18. CE81D31 $V_{OUT}=1.05\text{ V}$
Different V_{IN} Load Regulation

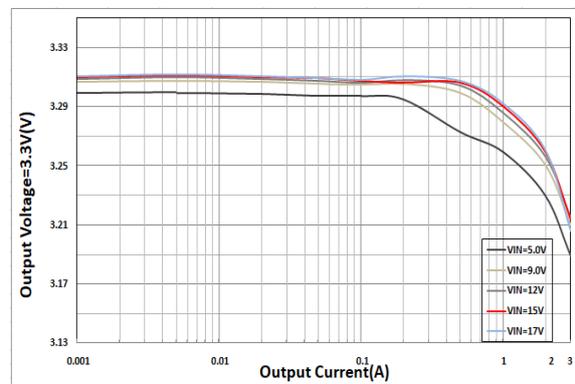


Figure19. CE81D31 $V_{OUT}=3.3\text{ V}$
Different V_{IN} Load Regulation

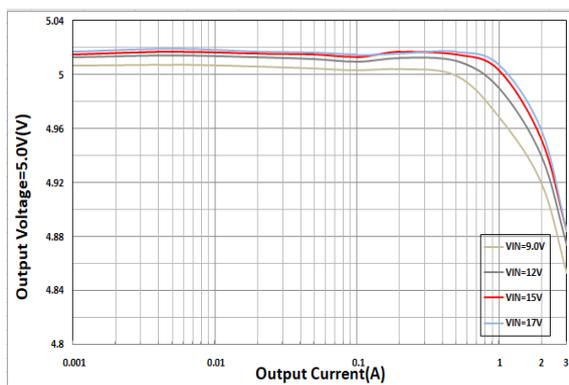


Figure20. Different V_{IN} Load Regulation,
 $V_{OUT}=5.0\text{ V}$

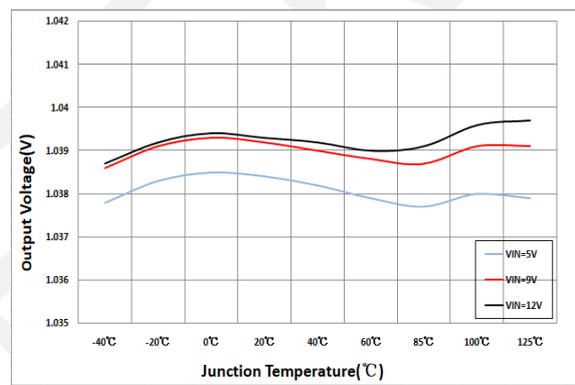
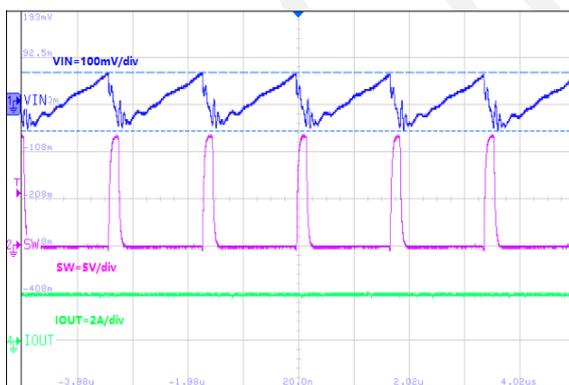
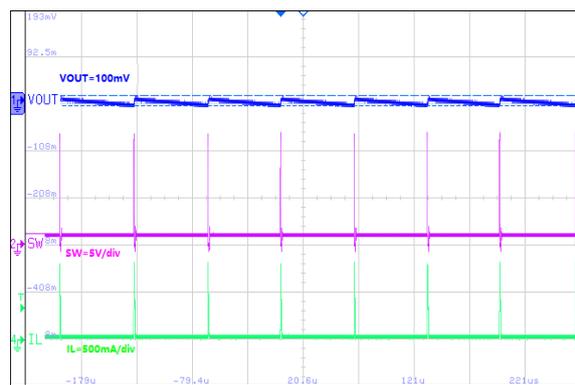


Figure21. Different Temperature V_{OUT} ,
 $V_{OUT}=1.05\text{ V}$



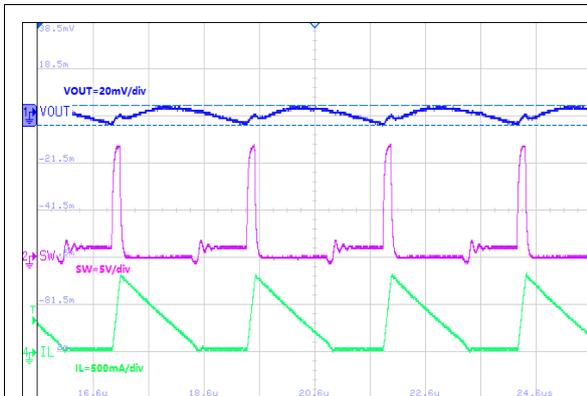
1 us/div
Figure22. CE81D31 Input Ripple



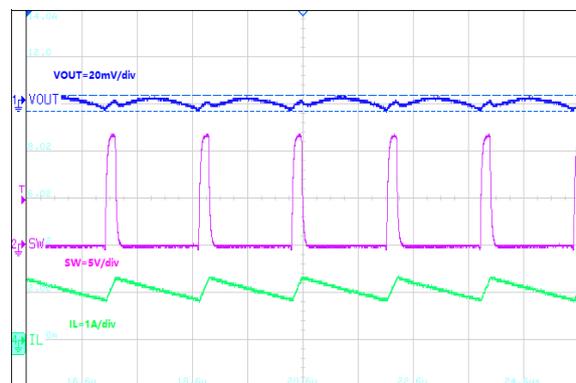
50 us/div
Figure23. CE81D31 $V_{OUT}=1.05\text{ V}$ Ripple
 $I_{OUT}=10\text{ mA}$

Application Curves(Continued)

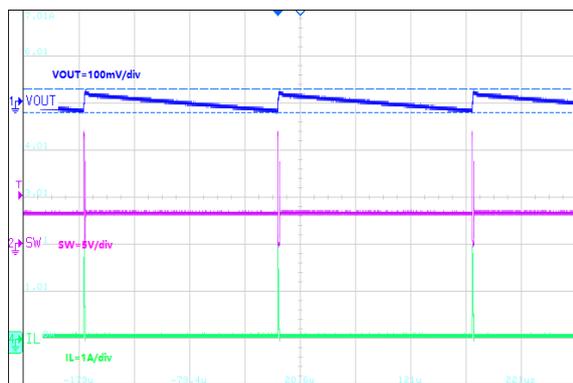
$V_{IN} = 12\text{ V}$ (unless otherwise noted)



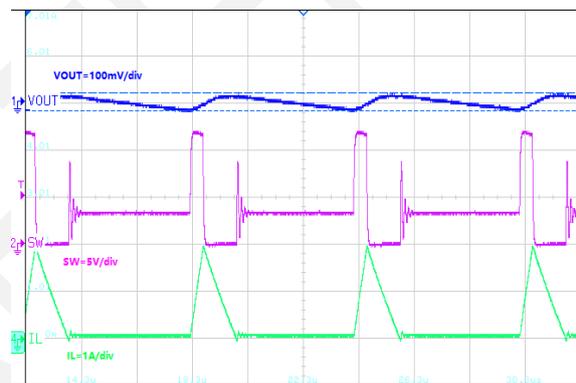
1 us/div
Figure24. CE81D31 $V_{OUT}=1.05\text{V}$ Ripple
 $I_{OUT}=250\text{ mA}$



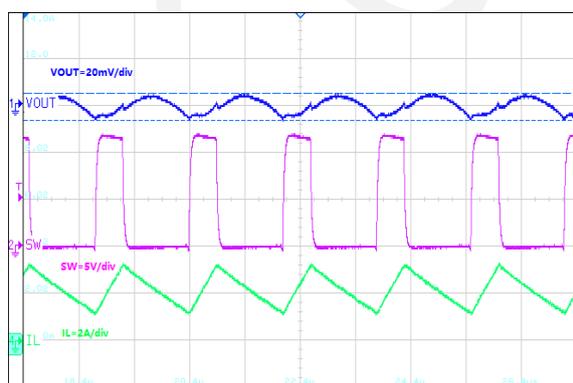
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Figure25. CE81D31 $V_{OUT}=1.05\text{ V}$ Ripple
 $I_{OUT}=2\text{ A}$



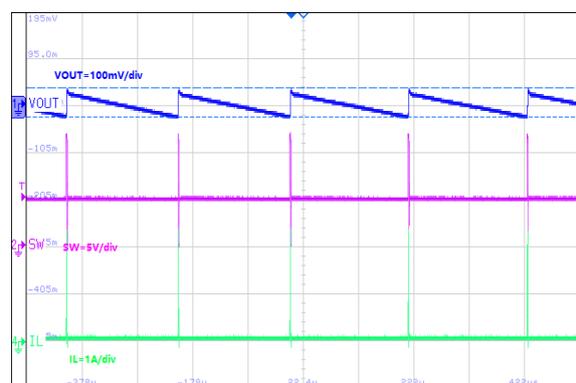
50 us/div
Figure26. CE81D31 $V_{OUT}=3.3\text{ V}$ Ripple
 $I_{OUT}=10\text{ mA}$



10 us/div
Figure27. CE81D31 $V_{OUT}=3.3\text{ V}$ Ripple
 $I_{OUT}=250\text{ mA}$



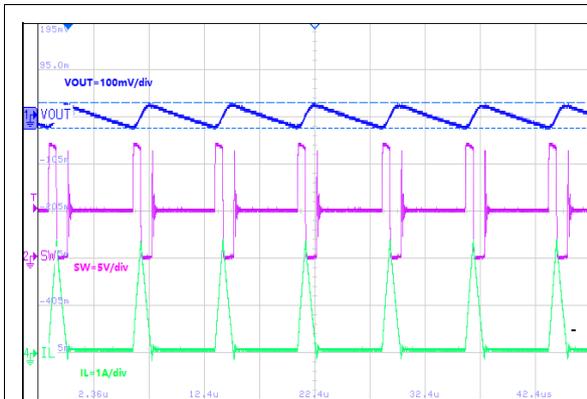
10 us/div
Figure28. CE81D31 $V_{OUT}=3.3\text{ V}$ Ripple
 $I_{OUT}=2\text{ A}$



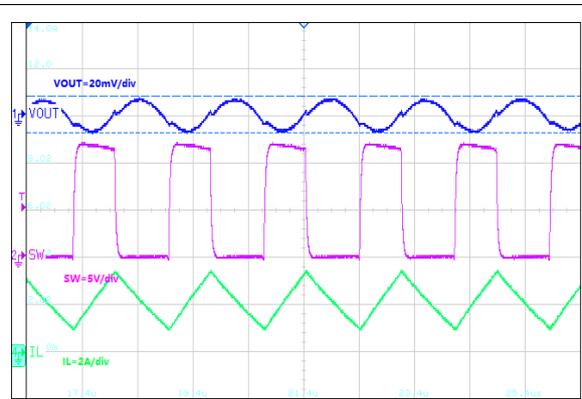
100 us/div
Figure29. CE81D31 $V_{OUT}=5.0\text{ V}$ Ripple
 $I_{OUT}=10\text{ mA}$

Application Curves(Continued)

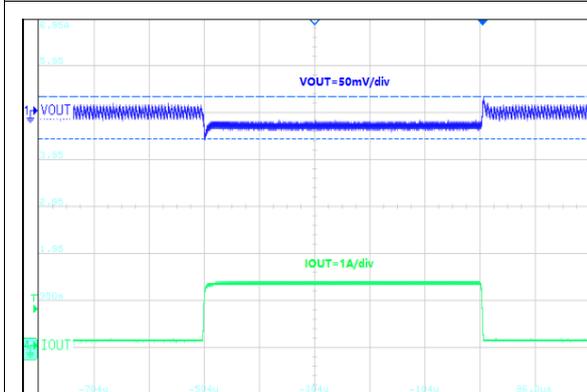
$V_{IN} = 12\text{ V}$ (unless otherwise noted)



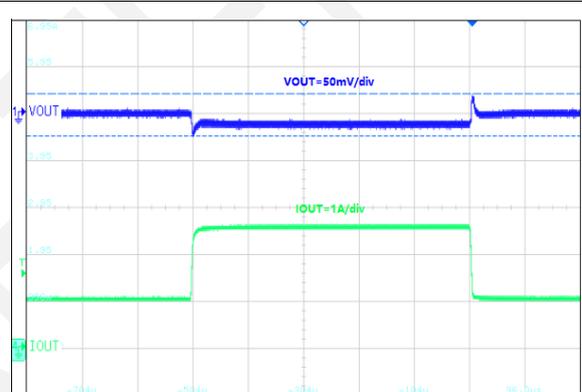
5 us/div
Figure30. CE81D31 $V_{OUT}=5.0\text{ V}$ Ripple
 $I_{OUT}=250\text{ mA}$



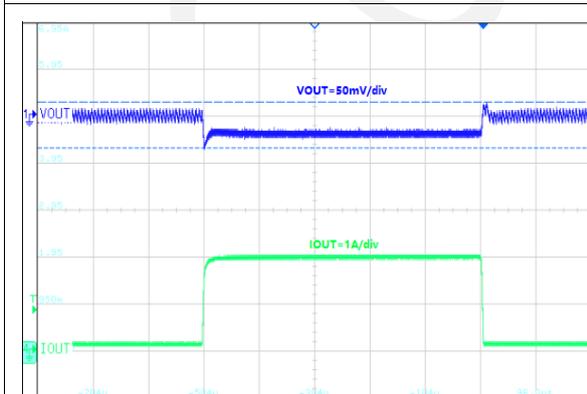
1 us/div
Figure31. CE81D31 $V_{OUT}=5.0\text{ V}$ Ripple
 $I_{OUT}=2\text{ A}$



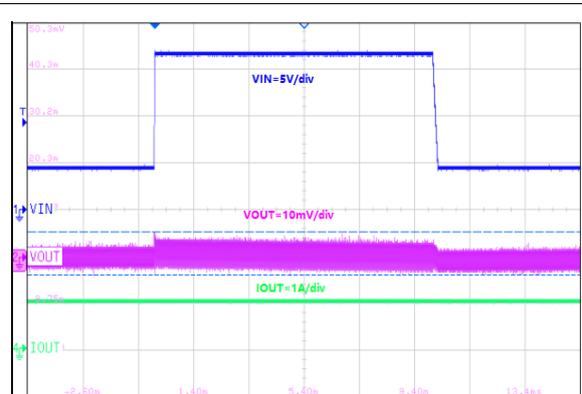
100 us/div
Figure32. CE81D31 Load Transient
 $V_{OUT}=1.05\text{ V}$, $I_{OUT} = 0.1\text{ A to }1.5\text{ A}$



100 us/div
Figure33. CE81D31 Load Transient
 $V_{OUT}=1.05\text{ V}$, $I_{OUT} = 1\text{ A to }2.5\text{ A}$



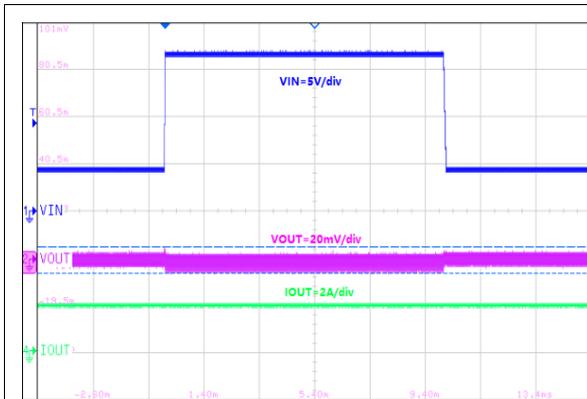
100 us/div
Figure34. CE81D31 Load Transient
 $V_{OUT}=1.05\text{ V}$, $I_{OUT} = 0.1\text{ A to }2\text{ A}$



2 ms/div
Figure35. CE81D31 Line Transient
 $V_{IN}=5\text{ V to }17\text{ V}$, $I_{OUT}=1\text{ A}$

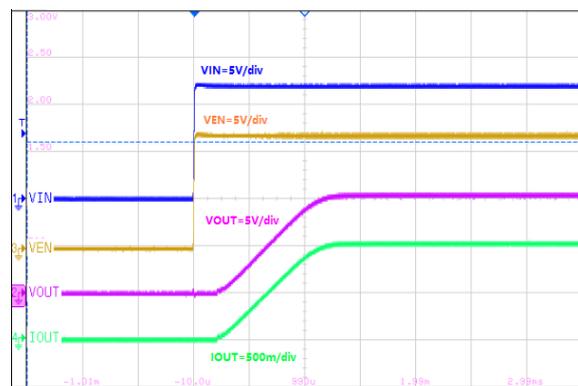
Application Curves(Continued)

$V_{IN} = 12\text{ V}$ (unless otherwise noted)



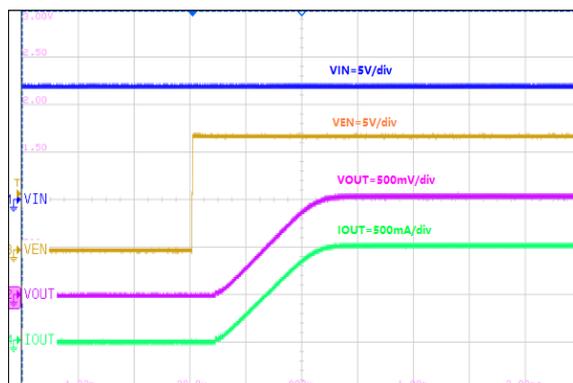
2 ms/div

Figure36. CE81D31 Line Transient
 $V_{IN}=5\text{ V to }17\text{ V}$, $I_{OUT}=2\text{ A}$



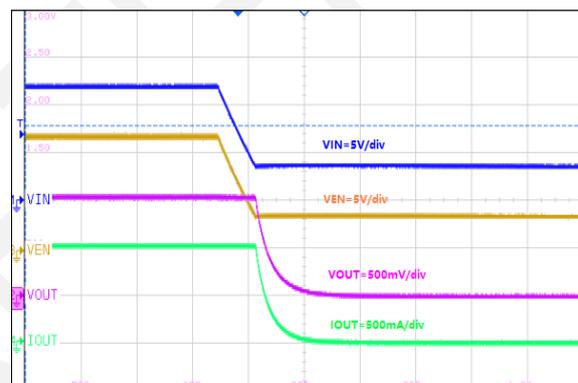
500 us/div

Figure37. CE81D31 Start-Up Relative to V_{IN}
 $I_{OUT}=1\text{ A}$



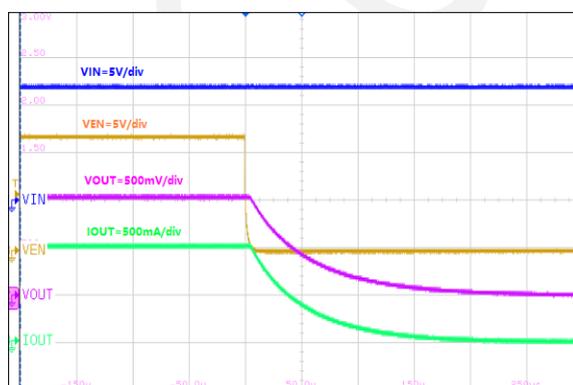
500 us/div

Figure38. CE81D31 Start-Up Relative to EN
 $I_{OUT}=1\text{ A}$



200 us/div

Figure39. CE81D31 Shutdown Relative to V_{IN}
 $I_{OUT}=1\text{ A}$

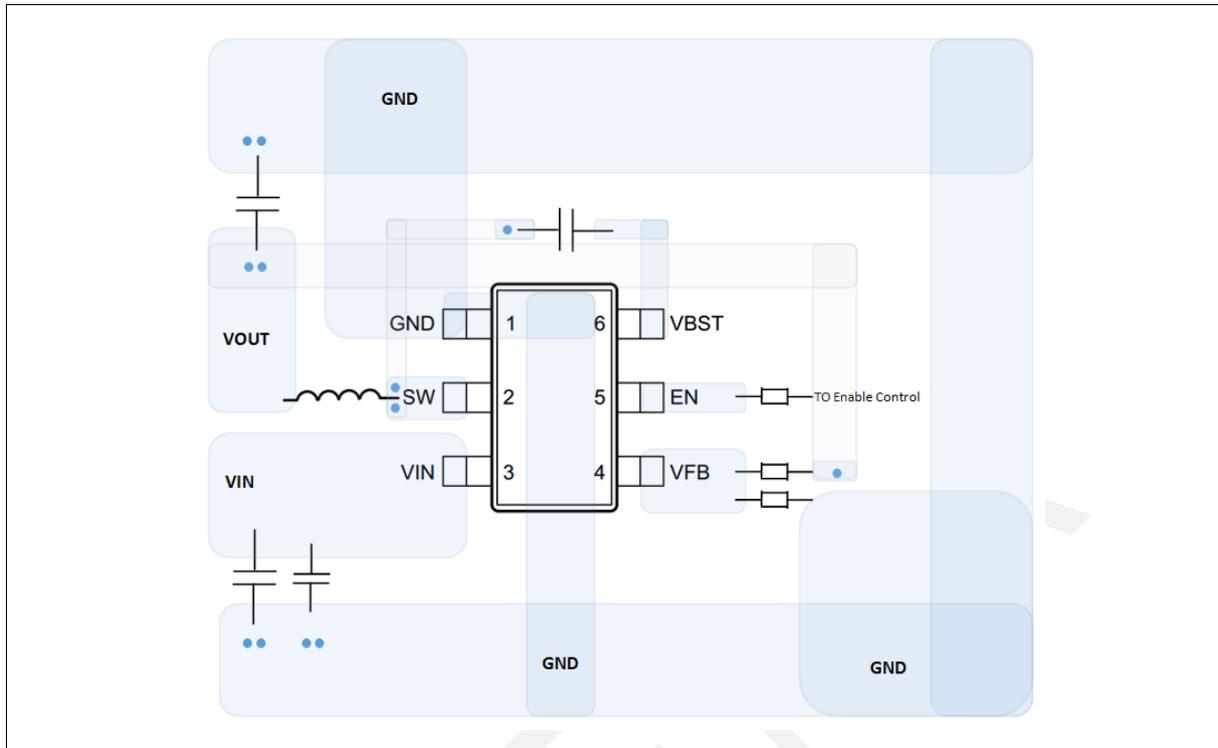


200 us/div

Figure40. CE81D31 Shutdown Relative to EN
 $I_{OUT}=1\text{ A}$

Layout

Layout Example



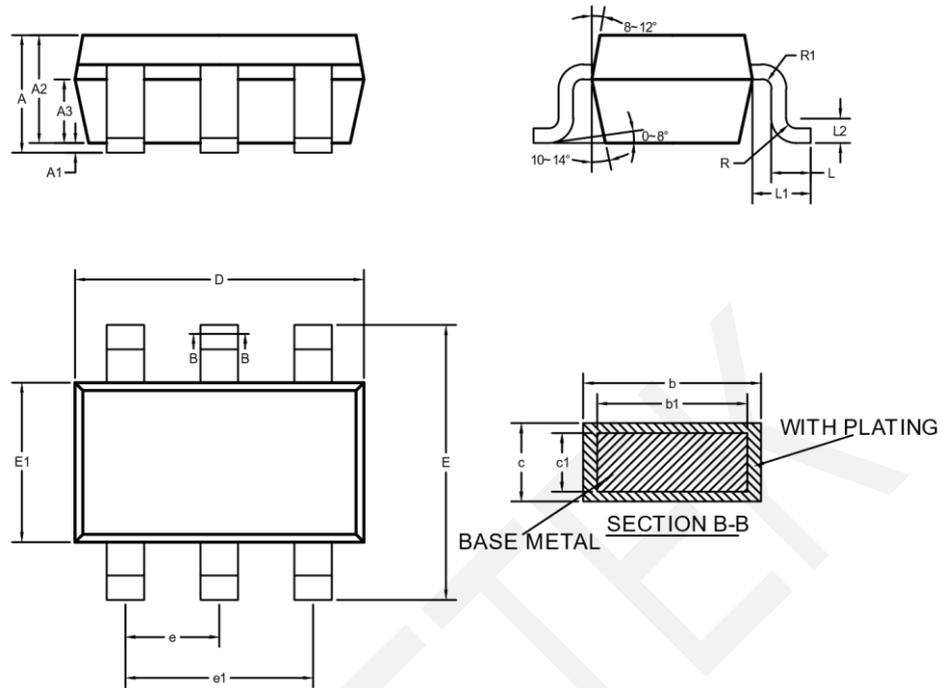
Note: Circuit diagram is for reference only.

Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance and better heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize-trace impedance.
3. Provide sufficient Vias for the input capacitor and output capacitor.
4. Keep the SW trace physically short and wide to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its-trace impedance.

Package Dimension

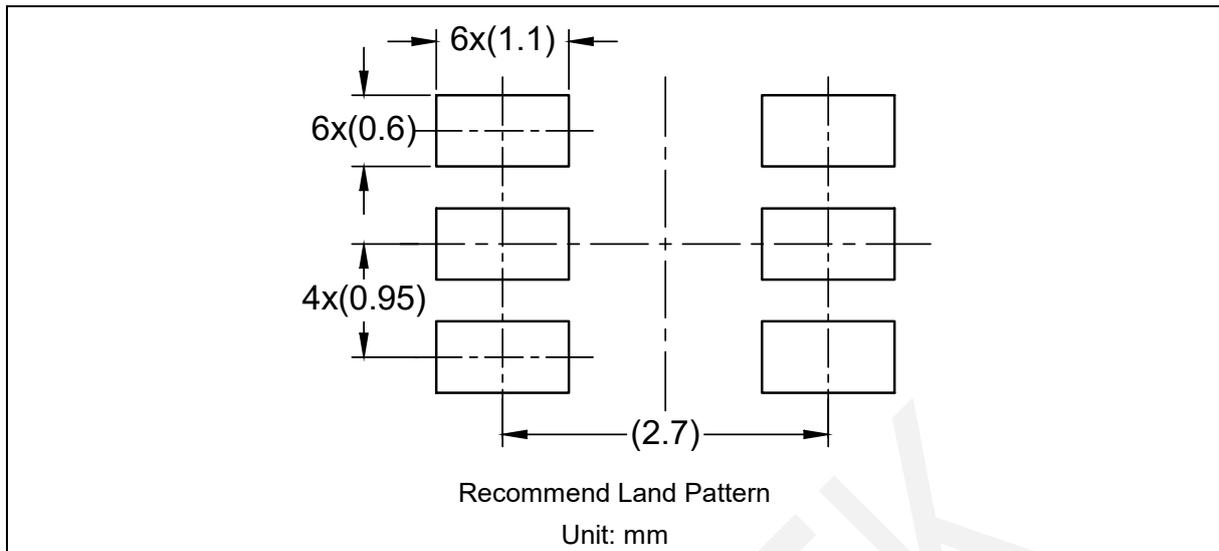
SOT23-6



Dimensions Table (Units: mm)

SYMBOL	MIN	NOM	MAX
A	—	—	1.250
A1	0	—	0.150
A2	0.750	—	1.200
A3	0.350	0.650	0.700
b	0.360	—	0.460
b1	0.350	0.380	0.430
c	0.130	—	0.200
c1	0.120	0.150	0.160
D	2.820	2.926	3.026
E	2.600	2.800	3.000
E1	1.500	1.626	1.726
e	0.900	0.950	1.000
e1	1.800	1.900	2.000
L	0.300	0.400	0.500
L1	0.590REF		
L2	0.250BSC		
R	0.050	—	0.200
R1	0.050	—	0.200

Recommend Land Pattern



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025.12.25	Official Version	LiuCong	Xie Lin Han	Xie Lin Han