CE65LH43ADJMQ - High Input Low I_Q 500mA ADJ Output LDO with PG

General Description

The CE65LH43ADJMQ is a low dropout with 500mA load ability with enable function LDO. It operates from 3V ~ 40V. The quiescent current is 12μA with no load. The devices feature integrated short-circuit and over-current protection. They are quite suitable for standby microprocessor control-unit systems, especially in automotive applications.

CE65LH43ADJMQ is available in the ESOP8 package and support ambient temperature range of -40 °C to 125 °C.

Features

- Input Voltage Range from 3V to 40V
- 500mA Load Current
- I_Q is 12μA Typical
- ADJ Output Voltage Range 1.8~20V
- Low Dropout is 620mV at 500mA Load @V_{OUT} = 5V
- Power-Good Feature is Available
- Over-Temperature Protection
- Current-Limit Protection'
- Automotive AEC-Q100 Grade 1 Qualified
  -- Ambient Temperature Range of -40 °C to 125 °C
  -- ESD HBM 2KV PASS
  -- ESD CDM 1.5KV PASS
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
CE65LH43ADJMQ	ESOP8 (4.9mm × 6.0mm)	Tape and Reel, 4K/Reel	3

Device information

CE 65LH43 ADJ M Q

ADJ Output Voltage		**M** Package		**Q** AEC-Q100 Qualified
ADJ	Output Voltage Adjustable.	M	ESOP8	Q: With AEC-Q100 Qualified

Applications

- Automotive Constant-Voltage Power Supply
- Automotive Infotainment and Cluster
- Automotive Power Supply for Body Electronics and Lighting

Pin Configuration

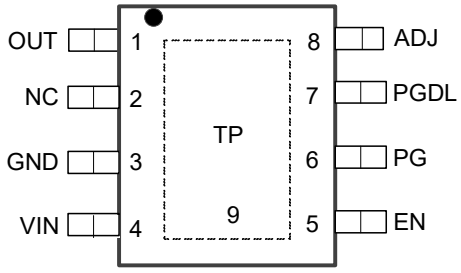

Figure1. Pin Configuration

Pin Function

Pin No.	Pin Name	Pin Function
1	OUT	Output Pin
2	NC	No Connect
3	GND	Ground Pin
4	VIN	Input Pin
5	EN	Enable Input Pin
6	PG	Power Good Pin
7	PGDL	PG Delay Pin
8	ADJ	Set the Output Voltage
9	TP	Thermal Pad, Floating or Connect to GND

Block Diagram

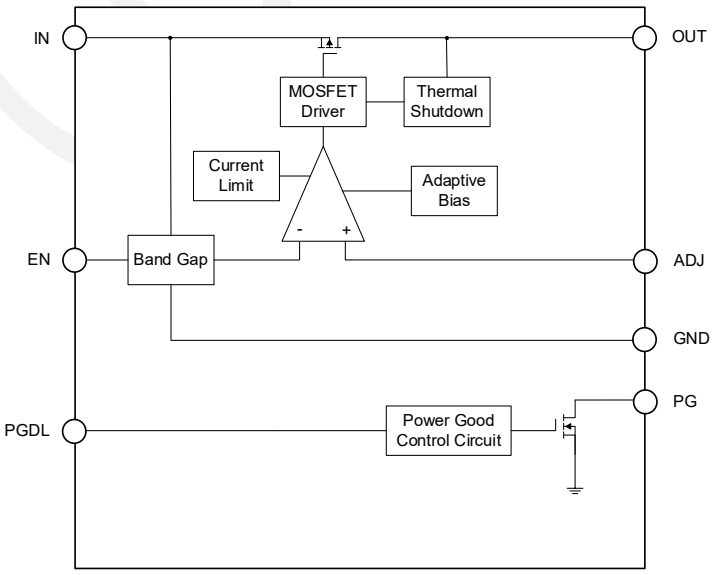

Figure2. Functional Block Diagram

Functional Description

Input Capacitor

A 1μF~10μF ceramic capacitor is recommended to connect between V_{IN} and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both V_{IN} and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1uF to 10uF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Enable

The CE65LH43ADJMQ delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Dropout Voltage

The CE65LH43ADJMQ uses a PMOS pass transistor to achieve low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} - V_{OUT}) approaches dropout operation.

Adjustable Output Voltage (ADJ)

One can select an output voltage between 1.8V to 20V by using an external resistor divider. Calculate the output voltage using the following equation, where V_{ADJ} = 1.15V, R2 ≥ 100KΩ

$$\mathbf{V_{OUT} = V_{ADJ} \times (1 + R1 / R2)}$$

Power Good

TheCE65LH43ADJMQ provides an open-drain PG Pin. The PG pin is an open-drain output and should be connected to V_{OUT}. When V_{OUT} rises 93% of V_{OUT}, the PG Pin is pulled to high by V_{OUT}. When V_{OUT} falls to 89% of V_{OUT}, the PG Pin is pulled to 0V.The delay time (t_{PGDL}) can be defined by adding a capacitor(C_{PGDL}) on PGDL through below equation:

$$\mathbf{t_{PGDL} = C_{PGDL} \times 5.2V / 5uA}$$

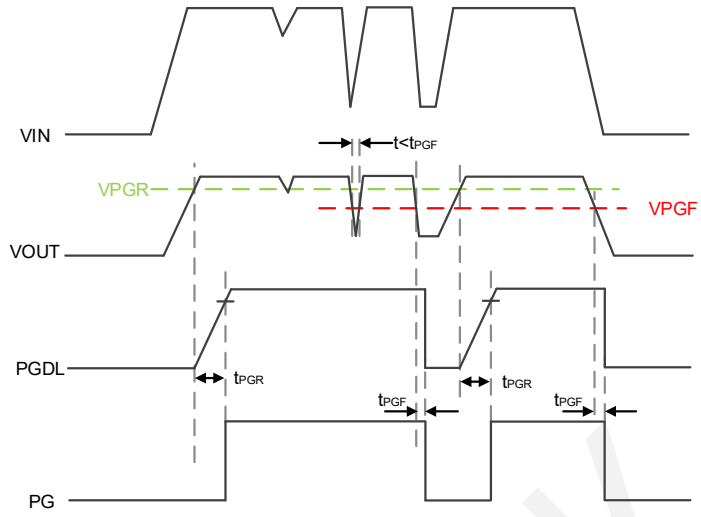

Figure3. Power Good Timing

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled.

Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} - V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 150°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance. For recommended operating condition specifications the maximum junction temperature is 150°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA} is layout dependent. The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance(θ_{JA}).

Current-Limit Protection

The CE65LH43ADJMQ provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

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ON/OFF Input Operation

The CE65LH43ADJMQ is turned on by setting the EN pin higher than V_{IH} threshold, and is turned off by pulling it lower than V_{IL} threshold. IN port needs to be powered on before the EN port. The recommended sequence diagram:

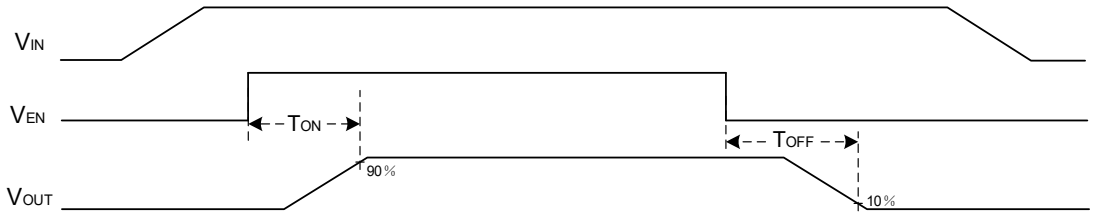


Figure4. Recommended sequence diagram

Absolute Maximum Ratings

Symbol	Rating		Value	Unit
V_{IN}	Input Voltage(1)		0~45 & V_{IN} > V_{EN}	V
V_{OUT}	Output Voltage		-0.3~25	V
V_{EN}	Chip Enable Input Voltage		-0.3~45	V
V_{ADJ}	FB Voltage		-0.3~6	V
V_{PG}	Power Good Voltage		-0.3~25	V
V_{PGDL}	Power Good Delay Voltage		-0.3~6	V
$T_{J(MAX)}$	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65~150	°C
V_{ESD} (2)	ESD Classification	Human Body Model	±2000	V
		Charged Device Model	±1500	V
I_{LU}(2)	Latch up Current Maximum Rating		±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: Refer to Electrical Characteristics and Application Information for Safe Operating Area and IN port needs to be powered on before the EN port.

Note2: This device series incorporates ESD protection and is tested by the following methods:

HBM tested per AEC-Q100-002(JEDEC JS-001);

CDM tested per AEC-Q100-011(JEDEC JS-002);

Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Thermal Characteristics

Symbol	Ratings	Value	Unit
$R_{\theta JA}$	Thermal Characteristics, Thermal Resistance, Junction-to-Air	69.5	°C/W
P_D	Max Power Dissipation @25°C	1.8	W

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3 to 40	V
I_{OUT}	Output Current	0 to 500	mA
T_A	Operating Ambient Temperature	-40 to 125	°C
C_{IN}	Input Capacitor Value	1 to 10	μF
C_{OUT}	Output Capacitor Value	1 to 10	μF
R_{PG}	Pull-up Resistor of Power-Good	1 to 100	kΩ
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Electrical Characteristics

(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.) (3)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN} (4)	Operating Input Voltage		3.0		40	V
I_Q (5)	Quiescent Current	I_{OUT} = 0mA, T_A = 25°C		12	20	μA
I_{Q_OFF}	Standby Current	V_{EN} = 0V, T_A = 25°C		0.1	1	μA
V_{FB}	Feedback Voltage	I_{OUT} = 1mA,T_A = 25°C	1.132	1.15	1.167	V
		I_{OUT} = 1mA, T_A = -40~125°C	1.104	1.15	1.196	
Reg_{LINE} (8)	Line Regulation	V_{OUT} + 2V ≤ V_{IN} ≤ 40V, I_{OUT} = 10mA		0.01	0.1	%/V
Reg_{LOAD} (8)	Load Regulation	1mA ≤ I_{OUT} ≤ 500mA, V_{OUT} = 3.3V, T_A = 25°C		15	45	mV
V_{DROP} (6) (8)	Dropout Voltage	I_{OUT} = 500mA, V_{OUT} = 5V,		620	900	mV
		I_{OUT} = 500mA, V_{OUT} = 20V,		620	1200	
I_{LMT}	Current Limit	V_{IN} = V_{OUT} + 2V, C_{OUT} = 1μF		1000	1500	mA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.4			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”			0.3	V
PSRR (7)	Power Supply Rejection Ratio	f = 1kHz, V_{IN} = V_{OUT} + 2V, V_{OUT} = 20V， I_{OUT} = 20mA		70		dB
e_N (7)	Output Noise Voltage	V_{IN} = V_{OUT} + 2V, I_{OUT} = 1mA, f = 10Hz to 100KHz, C_{OUT} = 1μF		25* V_{OUT}		μVrms
V_{PG_R}	PG Rising Threshold	V_{OUT} / V_{OUT_SET}, When V_{OUT} Rising	89	93	97	%
V_{PG_F}	PG Falling Threshold	V_{OUT} / V_{OUT_SET}, When V_{OUT} Falling	85	89	93	%
t_{D_PGR}	PG Rising Delay	C_{PGDL} = 0nF		600	900	μs
t_{D_PGF}	PG Falling Delay	C_{PGDL} = 0nF	2	10		μs
T_{SD}	Thermal Shutdown Temperature (7)	Temperature Increasing from T_A = 25°C		155		°C
T_{HYS}	Thermal Shutdown Hysteresis (7)	Temperature Falling from T_{SD}		25		°C

Note3: Here V_{IN} means internal circuit can work normal. If $V_{IN} < V_{OUT}$, Output voltage follows V_{IN}(I_{OUT} = 1mA), circuit is safety.

Note4: The minimum operating voltage is 3.0V. $V_{DROP} = V_{IN(min)} - V_{OUT}$.

Note5: R2 needs to be greater than or equal to 100KΩ.

Note6: V_{DROP} FT test method: test the V_{OUT} voltage at $V_{SET} + V_{DROPMAX}$ with 500mA output current.

Note7: Guaranteed by design and characterization. not a FT item.

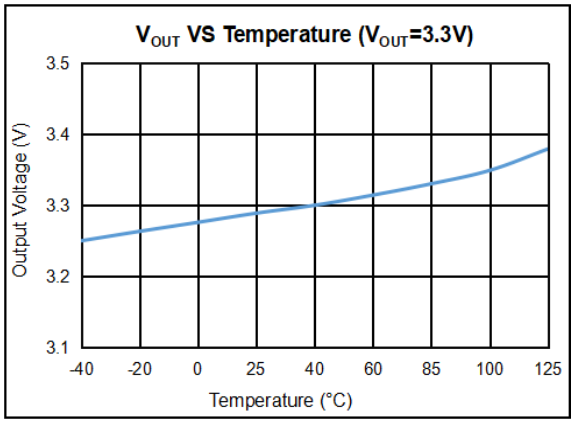
Note8: At high temperatures, the maximum load current can be calculated according to the following formula：

$$I_{OUT\_MAX} = (T_J - T_A) / R_{\theta JA} / (V_{IN} - V_{OUT})$$

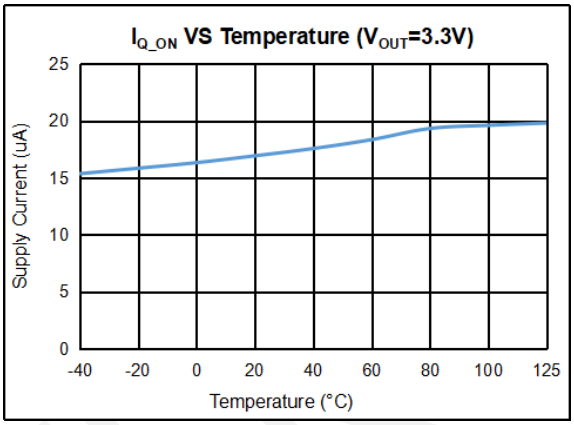
Typical Characteristics

V_{OUT} = 3.3V

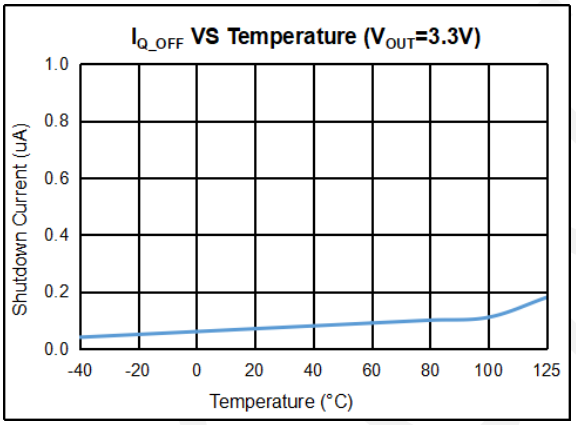
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



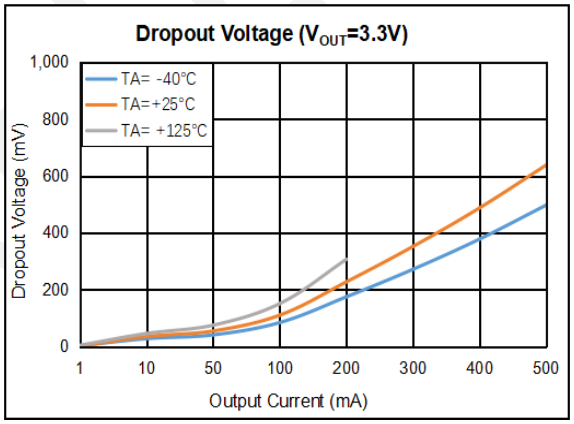
Output Voltage VS Temperature



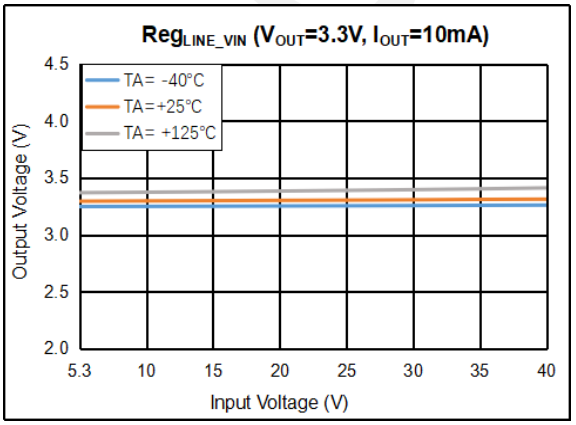
Supply Current VS Temperature



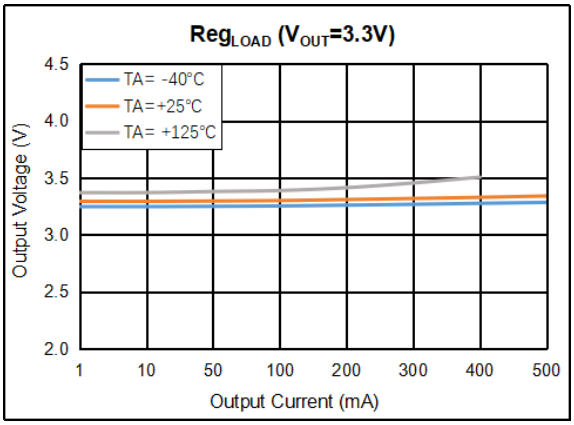
Shutdown Current VS Temperature



Dropout Voltage VS Output Current



Output Voltage VS Input Voltage

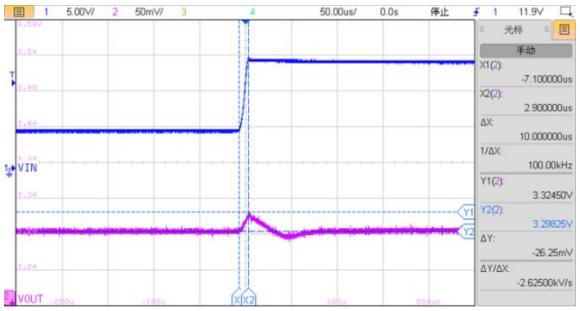


Output Voltage VS Output Current

Typical Characteristics (Continued)

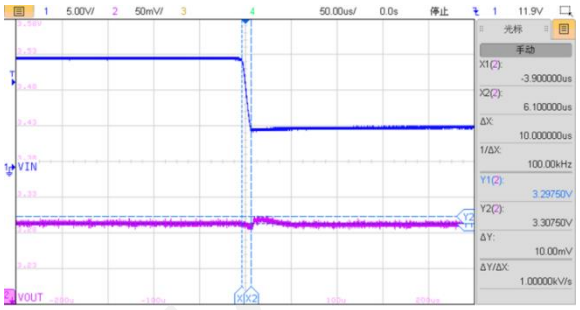
V_{OUT} = 3.3V

(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



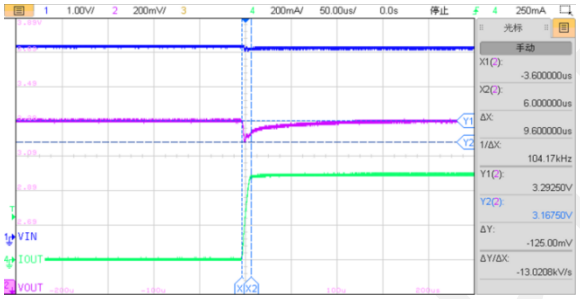
Line Transient Response

V_{IN} = 5.3V~15V, V_{OUT} = 3.3V, I_{OUT} = 10mA



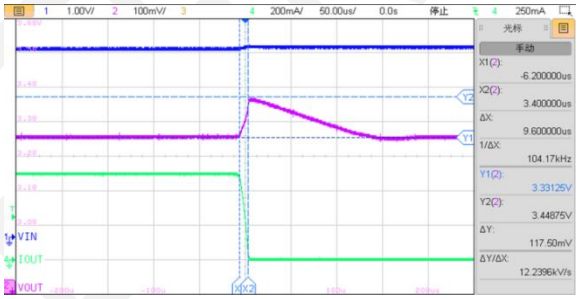
Line Transient Response

V_{IN} = 15V~5.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA



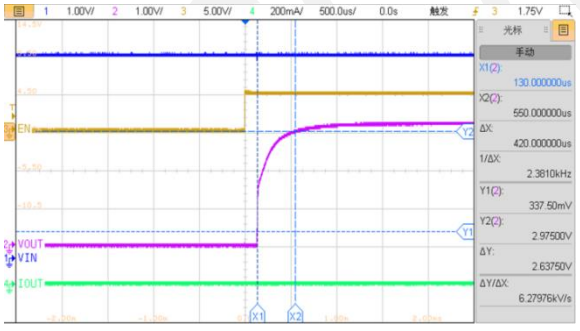
Load Transient Response

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 1mA~500mA



Load Transient Response

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 500mA~1mA



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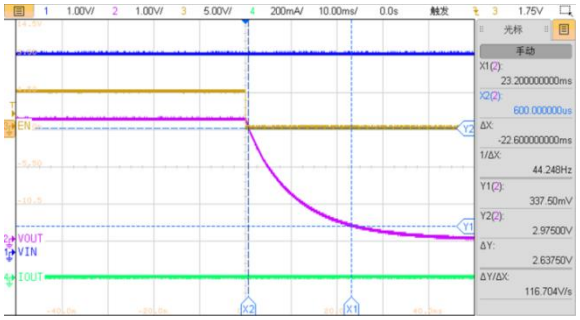
V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0mA



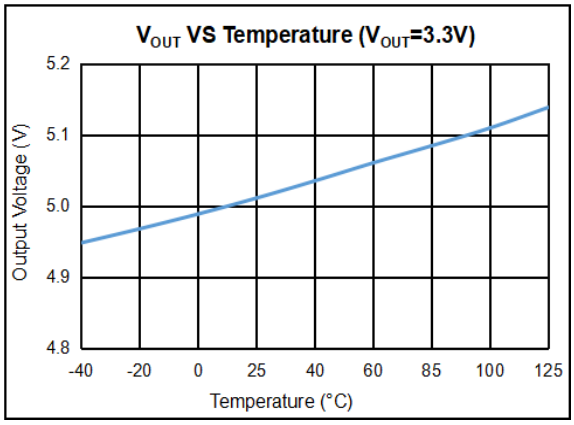
Toff

V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 0mA

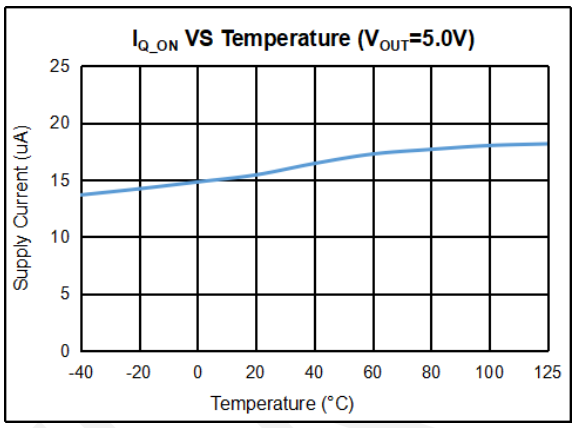
Typical Characteristics (Continued)

V_{OUT} = 5V

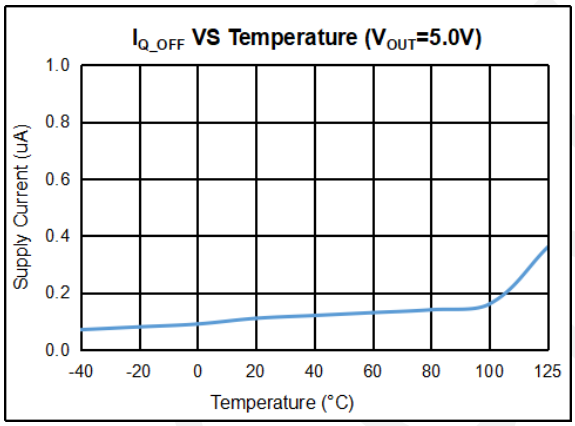
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



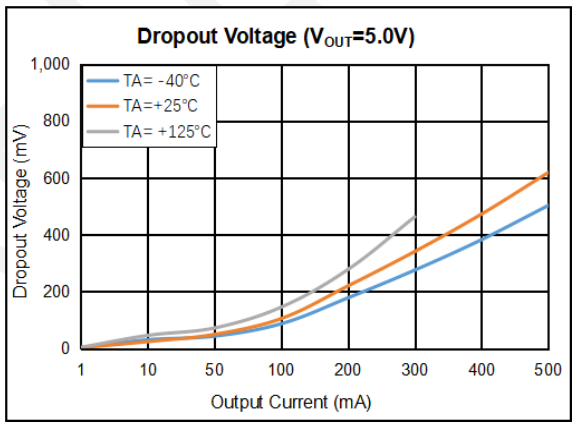
Output Voltage VS Temperature



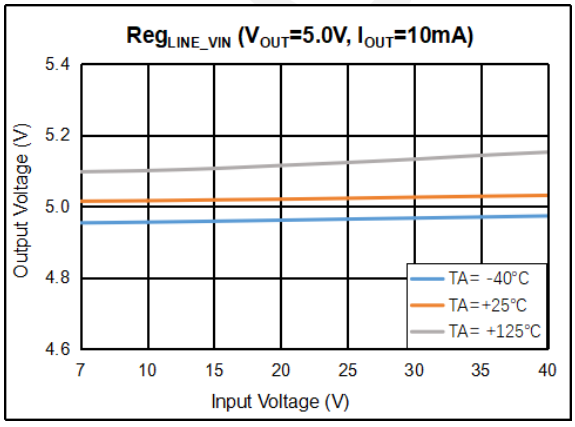
Supply Current VS Temperature



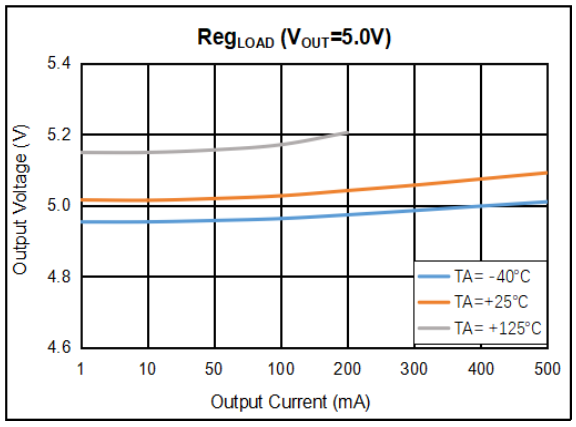
Shutdown Current VS Temperature



Dropout Voltage VS Output Current



Output Voltage VS Input Voltage

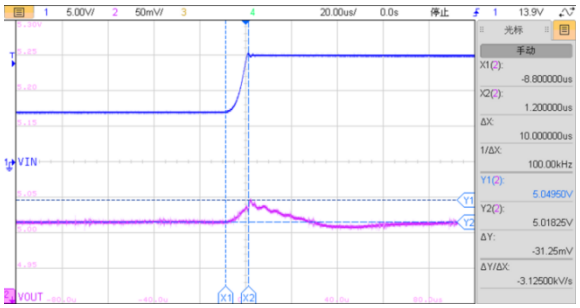


Output Voltage VS Output Current

Typical Characteristics (Continued)

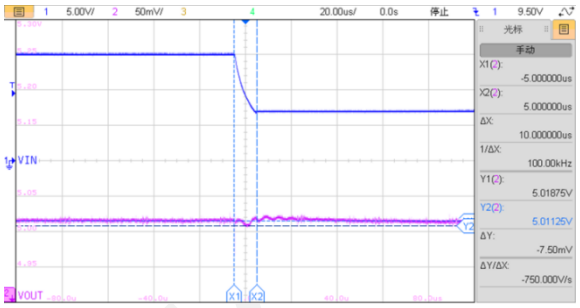
V_{OUT} = 5V

(V_{IN} =V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



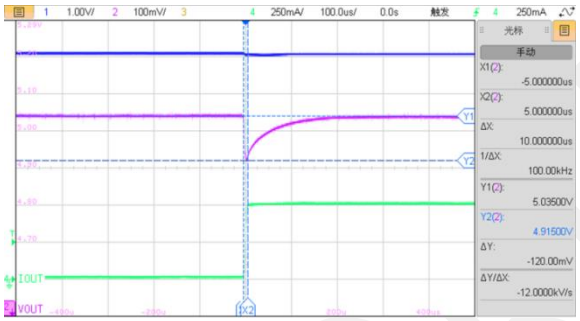
Line Transient Response

V_{IN} = 7V~15V, V_{OUT} = 5V, I_{OUT} = 10mA



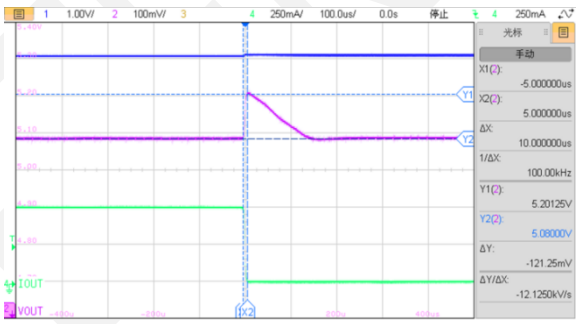
Line Transient Response

V_{IN} = 15V~7V, V_{OUT} = 5V, I_{OUT} = 10mA



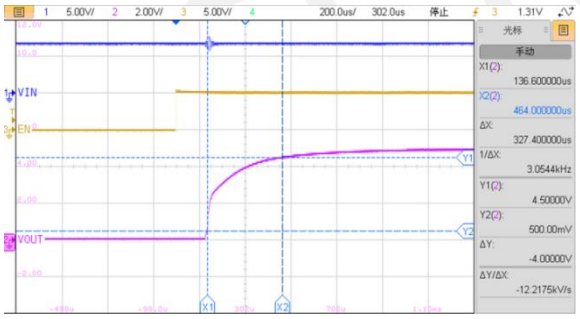
Load Transient Response

V_{IN} = 7V, V_{OUT} = 5V, I_{OUT} = 1mA~500mA



Load Transient Response

V_{IN} = 7V, V_{OUT} = 5V, I_{OUT} = 500mA~1mA



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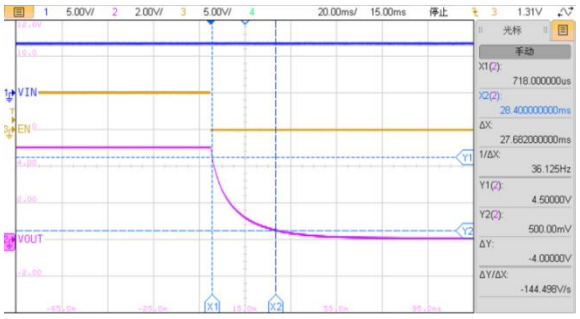
V_{IN} = 7V, V_{OUT} = 5V, I_{OUT} = 0mA



Toff

V_{IN} = 7V, V_{OUT} = 5V, I_{OUT} = 0mA

Application Circuits

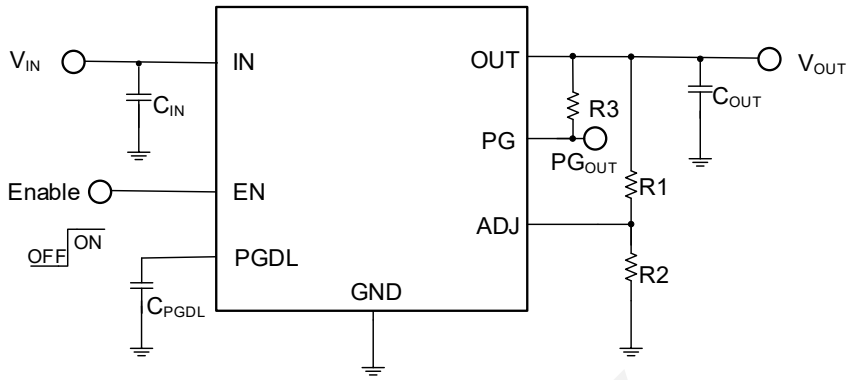


Figure5. Adjustable Voltage Typical Application Circuit

Note8: V_{OUT} = 1.15V × (1 + R1 / R2), R2 ≥ 100KΩ.

Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Do not place a thermal via directly beneath the thermal pad. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

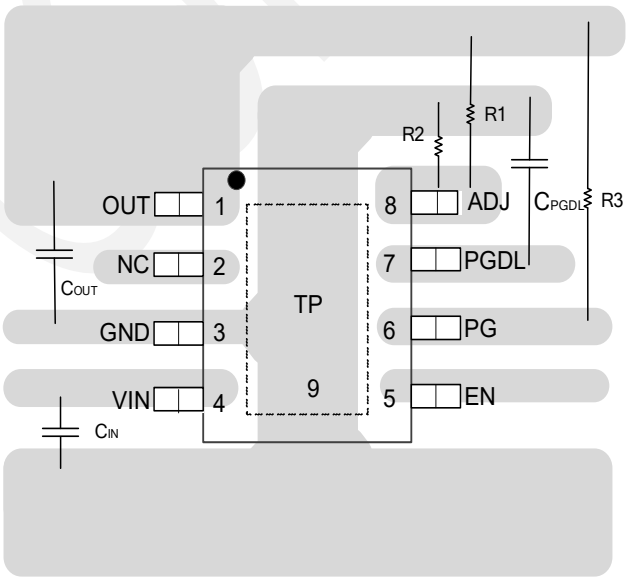
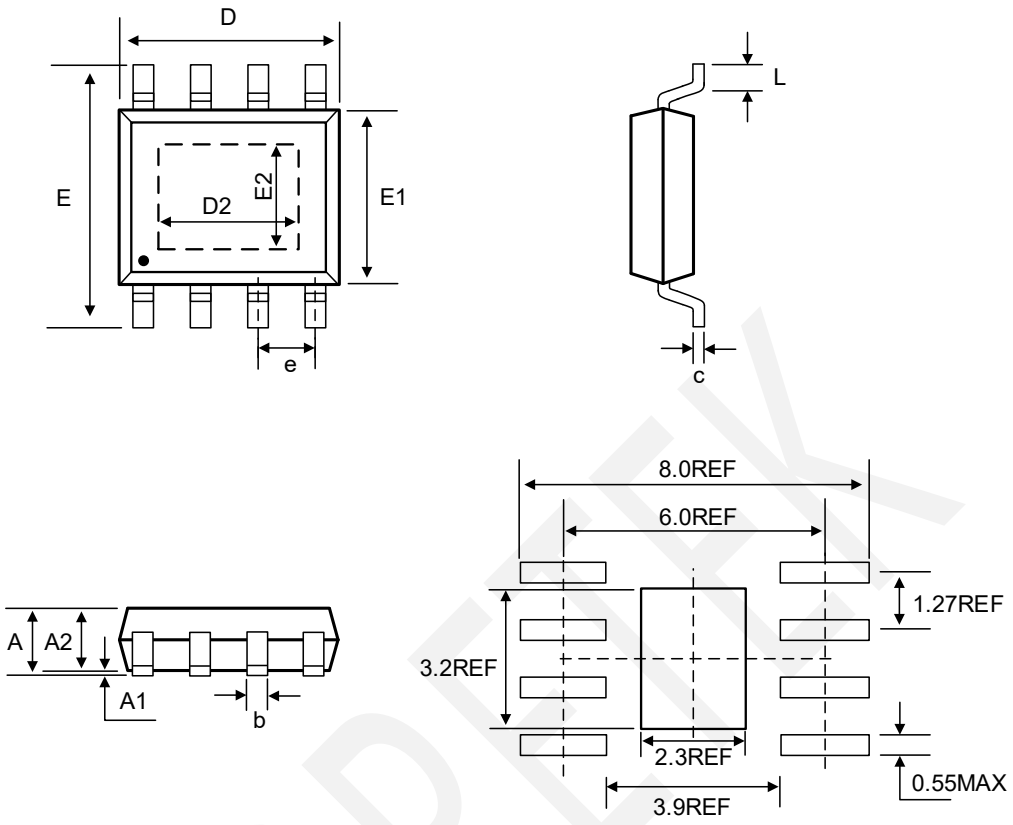


Figure6. Layout Guidelines

Package Dimension

ESOP8 (4.9mm × 6.0mm)



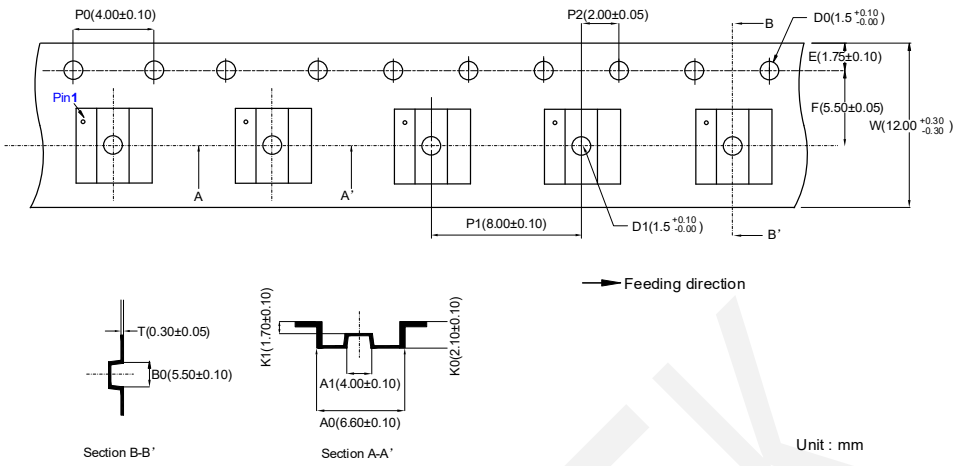
COMMON DIMENSIONS

(Unit: mm)

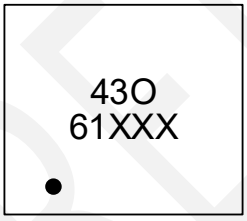
SYMBOL	MIN	NOM	MAX
A	-	-	1.90
A1	0.00	-	0.30
A2	1.20	1.40	1.60
b	0.35	-	0.47
c	0.15	-	0.27
D	4.70	4.90	5.10
E	5.80	6.00	6.20
D2	3.00	3.25	3.50
E1	3.70	3.90	4.10
E2	2.10	2.30	2.50
e	1.27BSC		
L	0.35	0.60	0.85

Tape Information

ESOP8 (4.9mm × 6.0mm)



Marking Information



43O = Part Number

65XXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-09-15	Preliminary Version	Tu guozhu	Gu jie, Liu xiaomin	Liu jiaying
0.1	2024-11-29	Update EC table and Package Dimension	Wang anran	Gu jie, Liu xiaomin	Liu jiaying
1.0	2025-05-23	Update EC table and Typical Characteristics	Li zihao	Yang xiaoxu	Liu jiaying