CE61LH41XXYQ - High Input Very-Low I_Q 150mA LDO

General Description

The CE61LH41XXYQ is a low dropout with 150mA load ability with enable function LDO. It operates from 3V ~ 40V. The quiescent current is 5.5μA with no load. The devices feature integrated short-circuit and over-current protection. They are quite suitable for standby microprocessor control-unit systems, especially in automotive applications.

CE61LH41XXYQ is available in the DNF6 (2mm × 2mm) package.

Features

- Input Voltage Range from 3V to 40V
- 150mA Load Current
- I_Q is 5.5μA Typical
- Fixed Output Voltage are 3.3V, 5.0V etc
- Low Dropout is 220mV at 150mA Load@ V_{OUT} = 5V
- Over-Temperature Protection
- Current-Limit Protection
- Automotive AEC-Q100 Grade 1 Qualified
  -- Ambient Temperature Range of -40°C to 125°C
  -- ESD HBM 2KV PASS
  -- ESD CDM 1.5KV PASS
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
CE61LH41XXYQ	DFN6 (2mm × 2mm)	Tape and Reel, 3K/Reel	1

Device information

CE61LH41 XX Y Q

XX Output Voltage		**Y** Package		**Q** AEC-Q100 Qualified	
XX	Output X.X-V For example, 33 is 3.3V output	Y	DFN6	Q	With AEC-Q100 Qualified

Applications

- Automotive Constant-Voltage Power Supply
- Automotive Infotainment and Cluster
- Automotive Power Supply for Body Electronics and Lighting

Pin Configuration

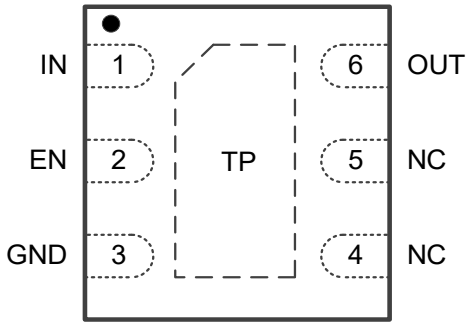


Figure1. Pin Configuration

Pin Function

Pin No.	Pin Name	Pin Function
1	IN	Input Pin
2	EN	Enable Input Pin, Active “H”
3	GND	Ground Pin
4,5	NC	No Connect
6	OUT	Output Pin
	TP	Thermal Pad, Recommend Floating or Connect to GND

Block Diagram

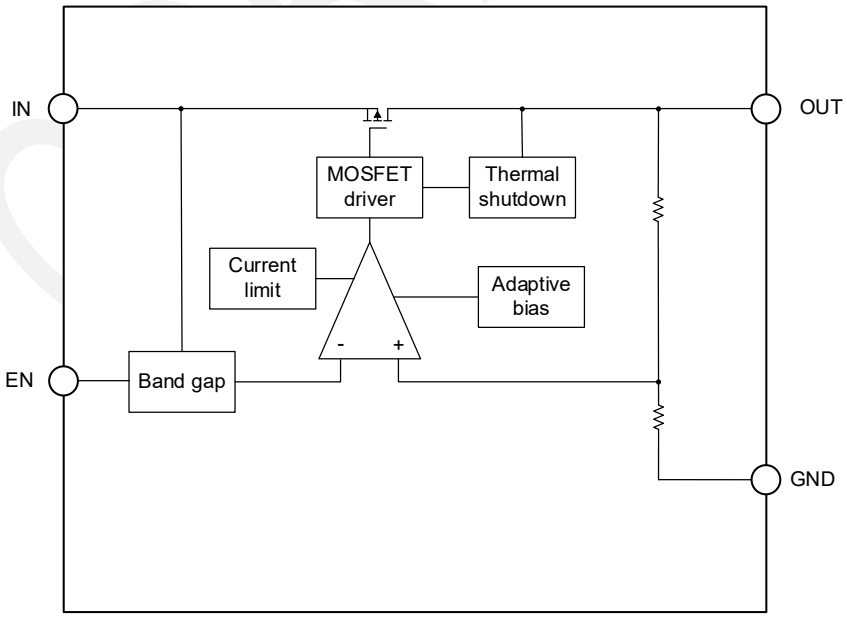


Figure2. Block Diagram

Functional Description

Input Capacitor

A 1μF~10μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Dropout Voltage

The CE61LH41XXYQ uses a PMOS pass transistor to achieve low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} - V_{OUT}) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 135°C, the output circuitry is again enabled.

Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} - V_{OUT}) voltage and the load current.

Current-Limit Protection

The CE61LH41XXYQ provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

ON/OFF Input Operation

The CE61LH41XXYQ is turned on by setting the EN pin higher than V_{IH} threshold, and is turned off by pulling it lower than V_{IL} threshold. IN port needs to be powered on before the EN port. The recommended sequence diagram:

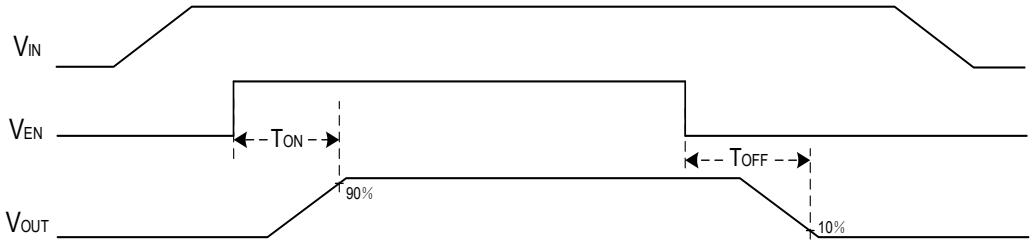


Figure3. Recommended sequence diagram

Absolute Maximum Ratings

Symbol	Rating		Value	Unit
V_{IN} (1)	Input Voltage		-0.3~45 & V_{IN} > V_{EN}	V
V_{EN}	EN Voltage		-0.3~12	V
V_{OUT}	Output Voltage		-0.3~18	V
$T_{J(MAX)}$ (2)	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65~150	°C
V_{ESD} (3)	ESD Classification	Human Body Model	±2000	V
		Charged Device Model	±1500	V
L_U (3)	Latch up Current Maximum Rating		±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: Refer to Electrical Characteristics and Application Information for Safe Operating Area and IN port needs to be powered on before the EN port.

Note2: When T_J > 125°C, there will be a large deviation in voltage accuracy.

Note3: This device series incorporates ESD protection and is tested by the following methods:

HBM tested per AEC-Q100-002(JEDEC JS-001);

CDM tested per AEC-Q100-011(JEDEC JS-002);

Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	DNF6	Thermal Characteristics, Thermal Resistance, Junction-to-Air	83.3	°C/W
P_D	DNF6	Max Power Dissipation @25°C	1.5	W

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3 to 40	V
V_{EN}	EN Voltage	3 to 10	V
I_{OUT}	Output Current	0 to 150	mA
T_A	Operating Ambient Temperature	-40 to 125	°C
C_{IN}	Input Capacitor Value	1 to 10	μF
C_{OUT}	Output Capacitor Value	1 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Electrical Characteristics

(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage (4)		3.0		40	V
V_{OUT}	Output Voltage Accuracy	I_{OUT} = 1mA, T_A = 25°C	-2.0		+2.0	%
		I_{OUT} = 1mA, T_A = -40~125°C	-3.5		+3.5	
I_Q	Quiescent Current	I_{OUT} = 0mA, T_A = 25°C		5.5	10	μA
I_{Q_OFF}	Standby Current	V_{EN} = 0V, T_A = 25°C		0.1	1	μA
$Line_{REG}$	Line Regulation (7)	V_{OUT} + 2V ≤ V_{IN} ≤40V I_{OUT} = 10mA		0.01	0.05	%/V
$Load_{REG}$	Load Regulation (7)	1mA ≤ I_{OUT} ≤ 150mA, V_{OUT} = 5V V_{IN} = V_{OUT} + 2V		10	30	mV
V_{DROP}	Dropout Voltage (5) (7)	V_{OUT} = 3.3V, I_{OUT} = 150mA		280	400	mV
		V_{OUT} = 5V, I_{OUT} = 150mA		220	350	mV
I_{LMT}	Current Limit	V_{IN} = V_{OUT} + 2V	200	350	500	mA
PSRR	Power Supply Rejection Ratio (6)	f = 1kHz, V_{IN} =V_{OUT} + 2V, V_{OUT} = 5V, I_{OUT} = 20mA		70		dB
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.4			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”			0.4	V
e_N	Output Noise Voltage (6)	V_{IN} = V_{OUT} + 2V, I_{OUT} = 1mA, f = 10Hz to 100KHz,		45* V_{OUT}		μVrms
T_{TSD}	Thermal Shutdown Temperature (6)	Temperature Increasing from T_A = 25°C	135	155	170	°C
T_{HYS}	Thermal Shutdown Hysteresis (6)	Temperature Falling from T_{TSD}		20		°C

Note4: Here V_{IN} means internal circuit can work normal. If V_{IN} < V_{OUT}, Output voltage follows V_{IN}(I_{OUT} = 1mA), circuit is safety.

Note5: V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} + $V_{DROPMAX}$ with 150mA output current.

Note6: Guaranteed by design and characterization. not a FT item.

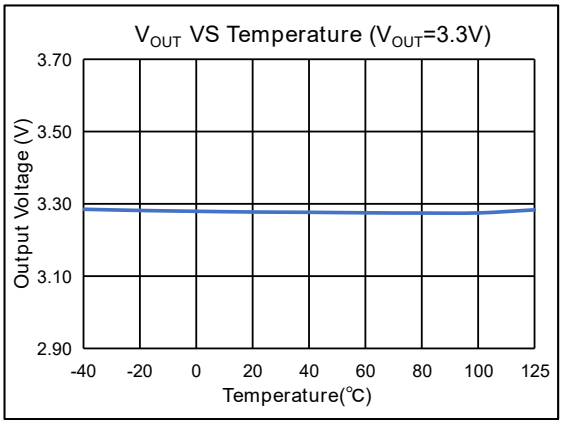
Note7: At high temperatures, the maximum load current can be calculated according to the following formula：

$$I_{OUT\_MAX} = (T_J - T_A) / R_{\theta JA} / (V_{IN} - V_{OUT})$$

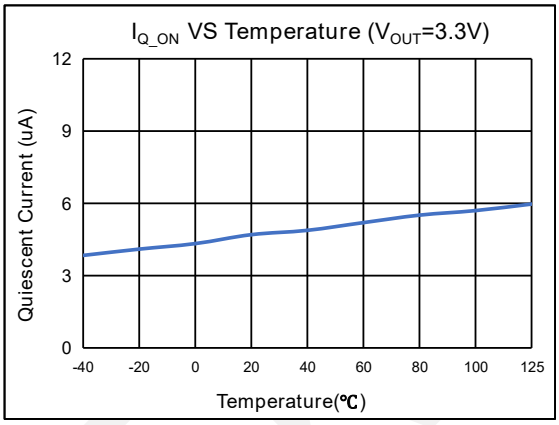
Typical Characteristics

V_{OUT} = 3.3V Version

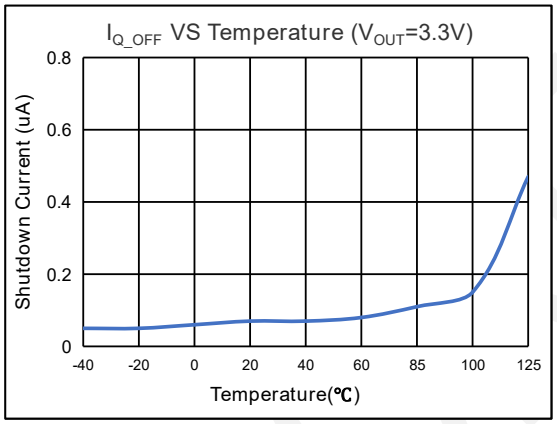
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



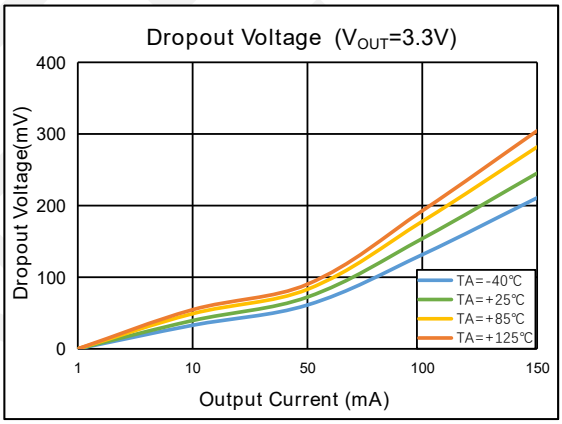
Output Voltage VS Temperature



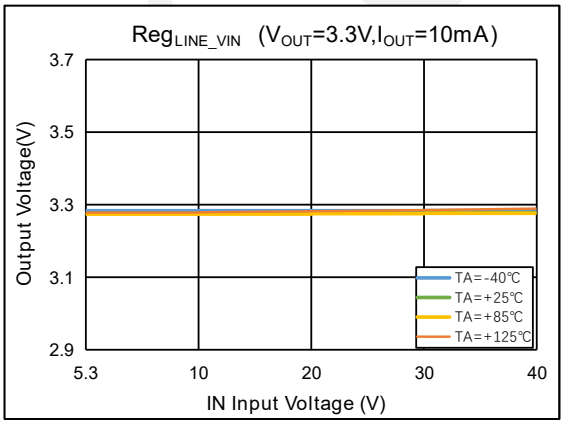
Supply Current VS Temperature



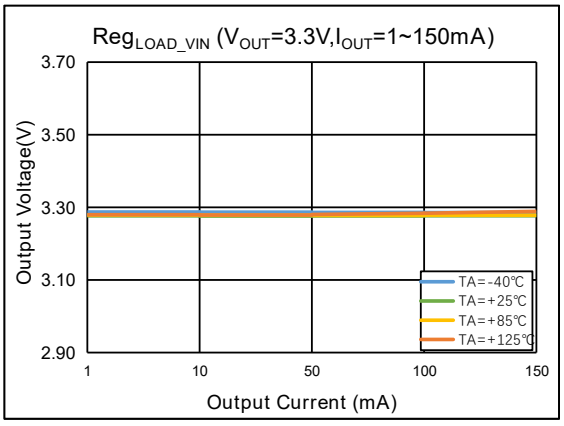
Shutdown Current VS Temperature



Dropout Voltage VS Output Current



Output Voltage VS Input Voltage

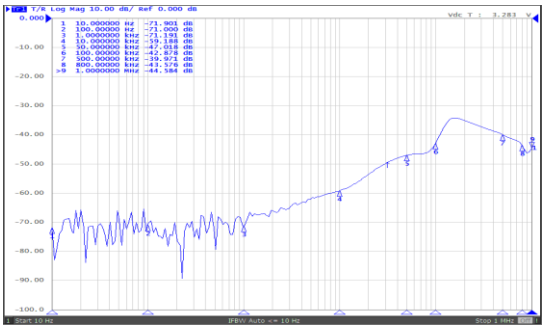


Output Voltage VS Output Current

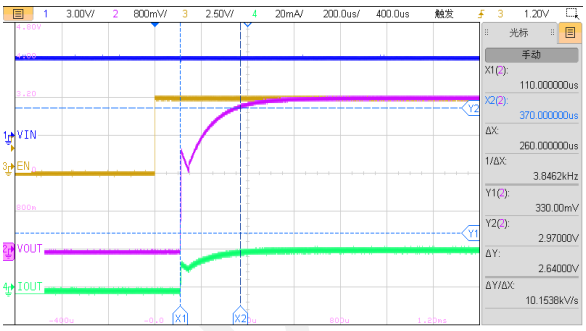
Typical Characteristics (Continued)

V_{OUT} = 3.3V Version

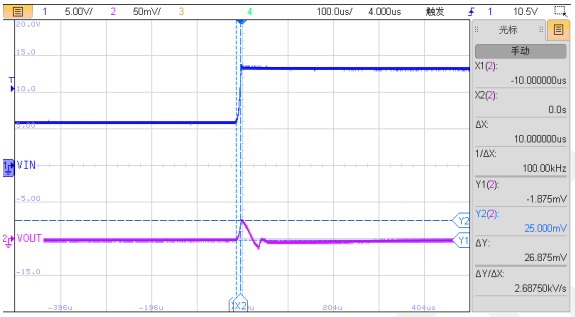
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



PSRR (I_{OUT} = 20mA)

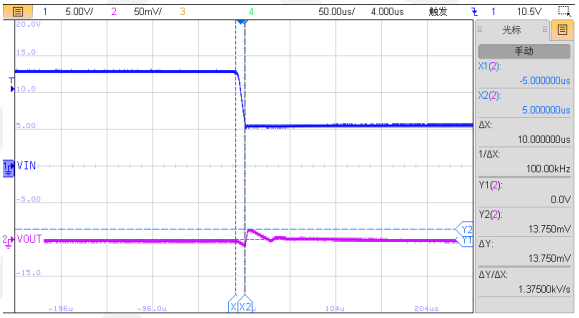


ton, V_{IN} = 5.3V, V_{OUT} = 3.3V, I_{OUT} = 0mA



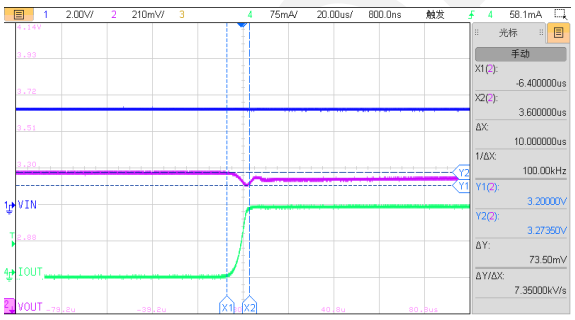
Line Transient Response

V_{IN} = 5.3V~13.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA



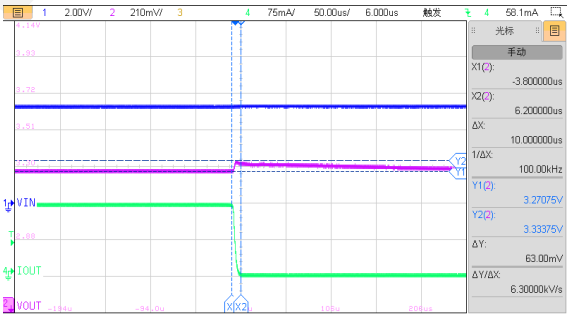
Line Transient Response

V_{IN} = 13.3V~5.3V, V_{OUT} = 3.3V, I_{OUT} = 10mA



Load Transient Response

V_{IN} = 5.3V, V_{OUT} = 3.3V, I_{OUT} = 1mA~150mA



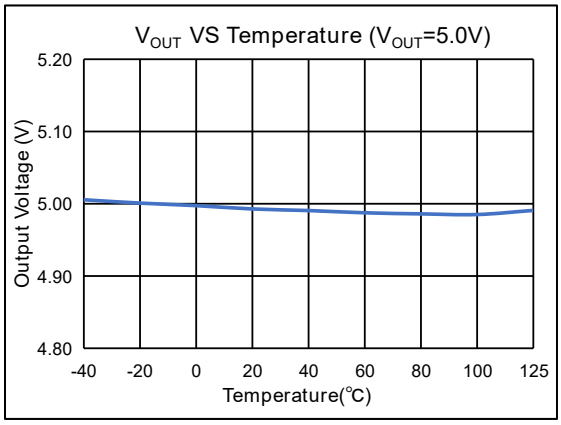
Load Transient Response

V_{IN} = 5.3V, V_{OUT} = 3.3V, I_{OUT} = 150mA~1mA

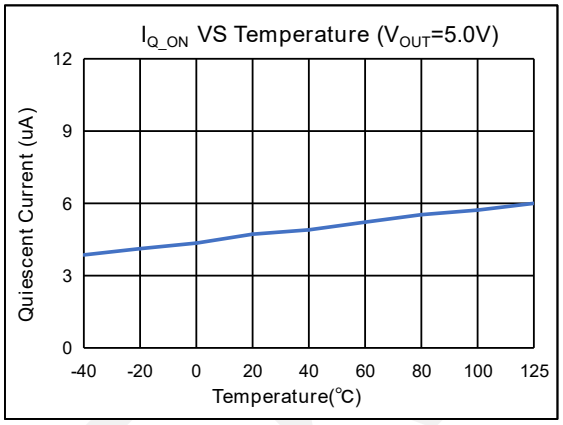
Typical Characteristics (Continued)

V_{OUT} = 5.0V Version

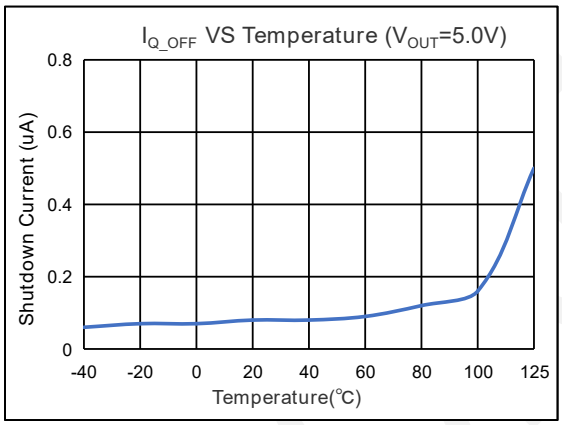
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



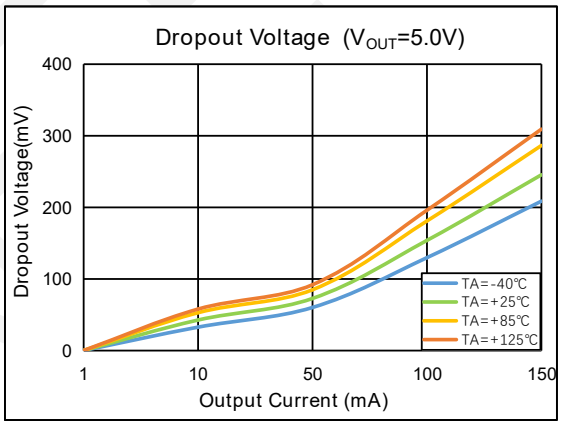
Output Voltage VS Temperature



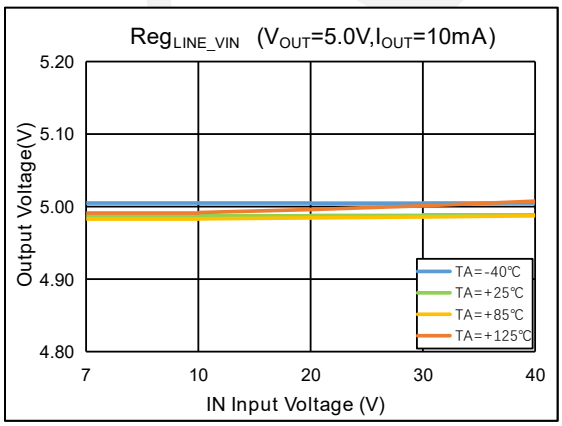
Supply Current VS Temperature



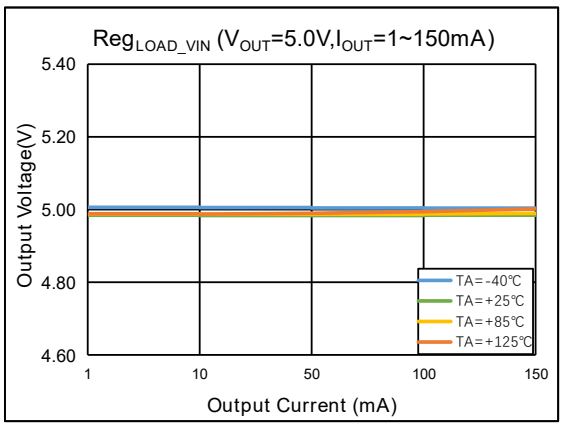
Shutdown Current VS Temperature



Dropout Voltage VS Output Current



Output Voltage VS Input Voltage

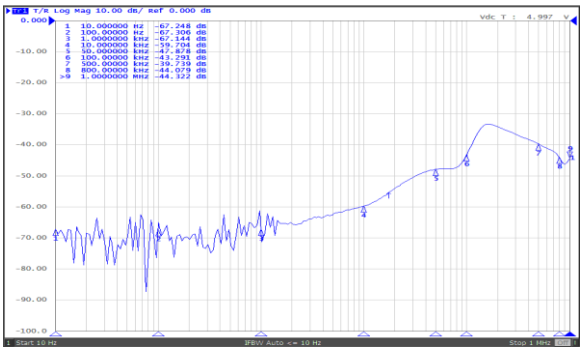


Output Voltage VS Output Current

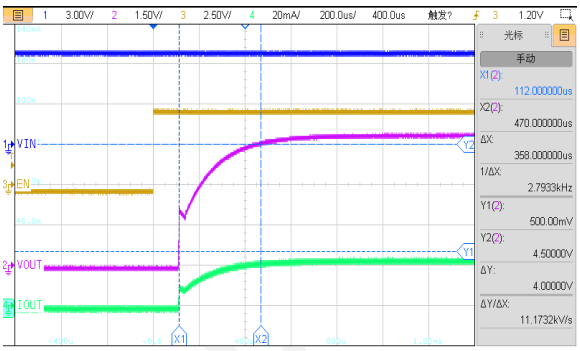
Typical Characteristics (Continued)

V_{OUT} = 5.0V Version

(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1.0μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)

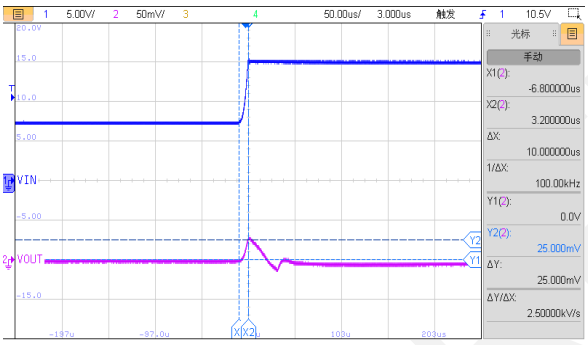


PSRR (I_{OUT} = 20mA)



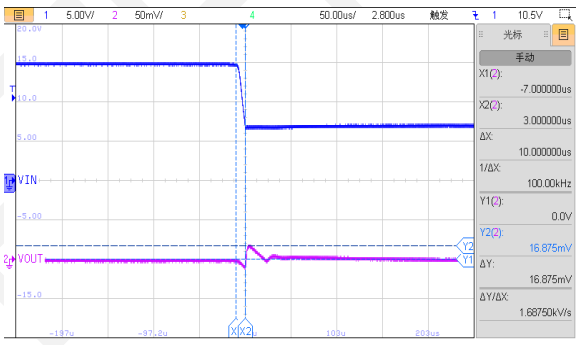
ton

V_{IN} = 5.3V, V_{OUT} = 3.3V, I_{OUT} = 0mA



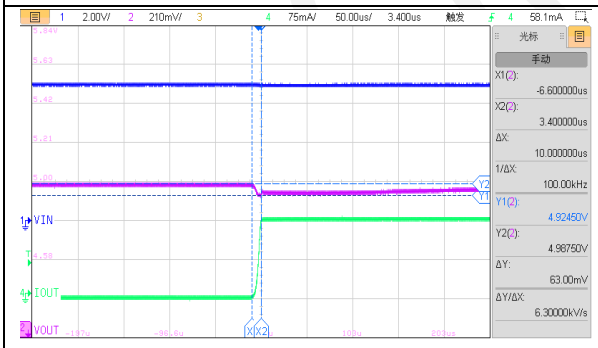
Line Transient Response

V_{IN} = 7.0V~15V, V_{OUT} = 5.0V, I_{OUT} = 10mA



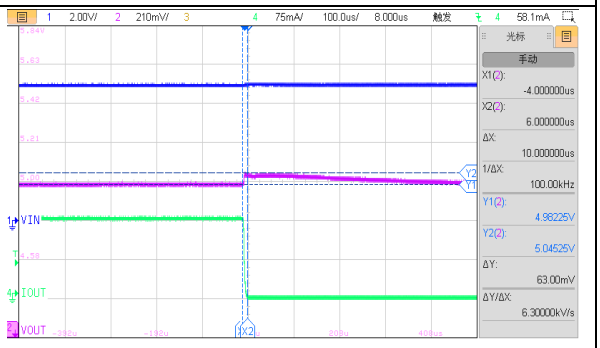
Line Transient Response

V_{IN} = 15V~7.0V, V_{OUT} = 5.0V, I_{OUT} = 10mA



Load Transient Response

V_{IN} = 7.0V, V_{OUT} = 5.0V, I_{OUT} = 1mA~150mA



Load Transient Response

V_{IN} = 7.0V, V_{OUT} = 5.0V, I_{OUT} = 150mA~1mA

Application Circuits

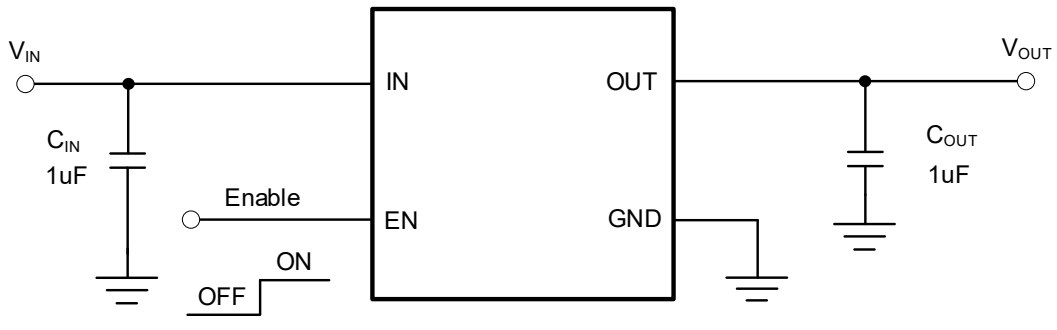


Figure4. Application Circuits

PCB Layout Guide

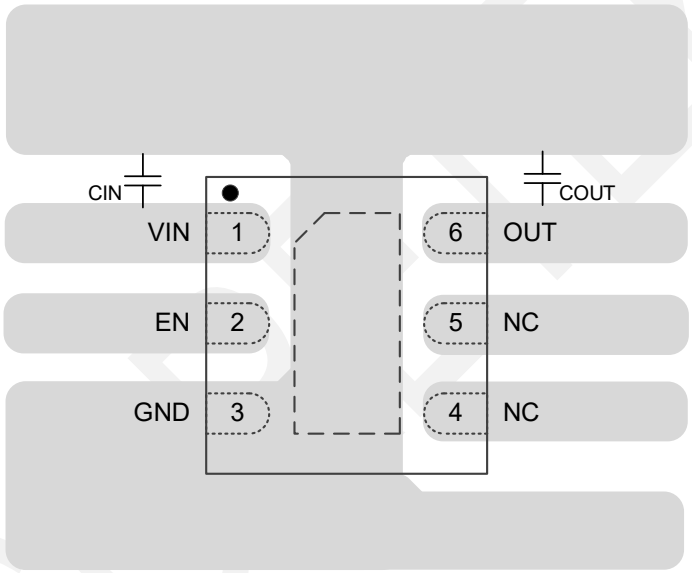
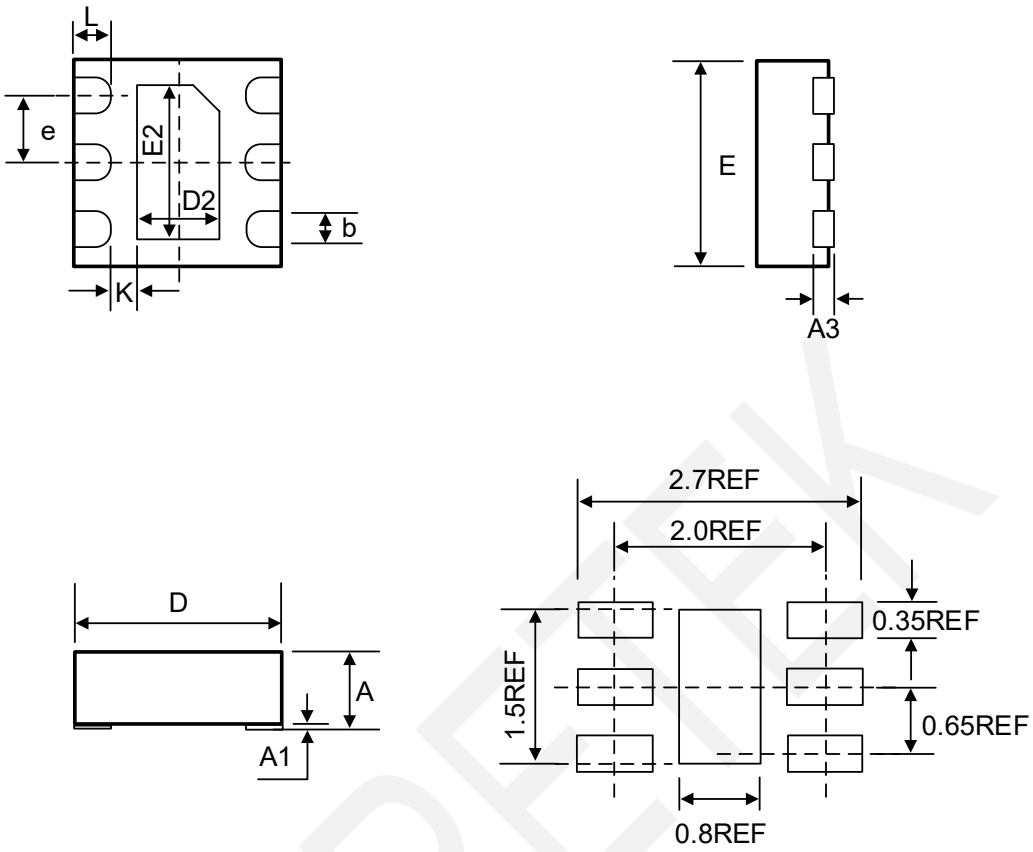


Figure5. PCB Layout Guide

Package Dimension

DNF6 (2mm × 2mm)



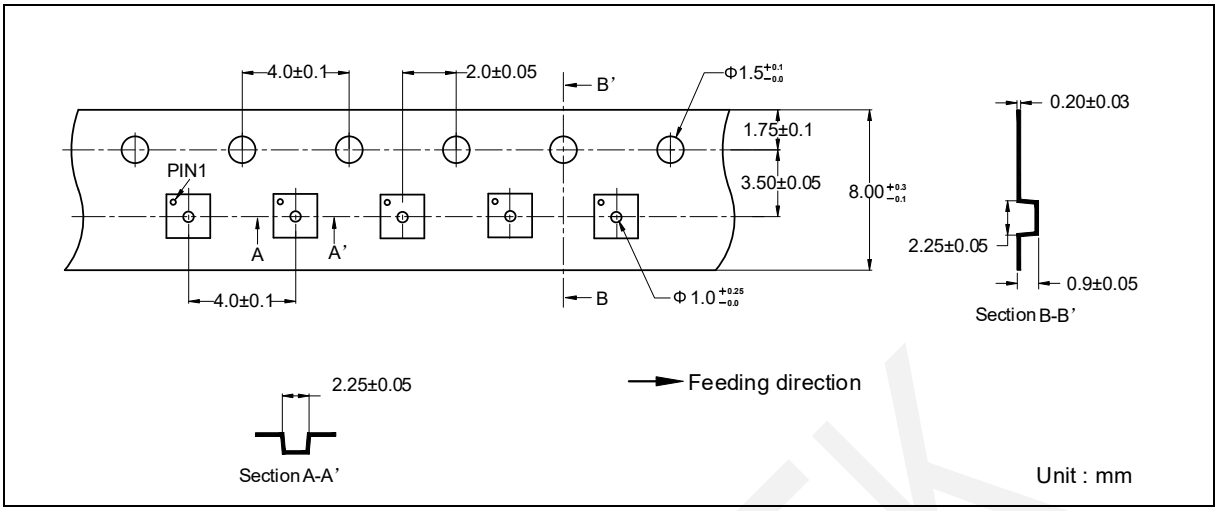
COMMON DIMENSIONS

(Unit: mm)

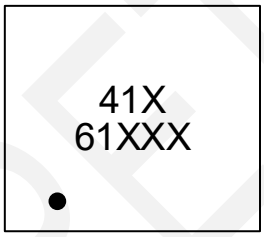
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.25	0.35	0.45
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.65	0.80	0.90
E2	1.35	1.50	1.60
e		0.65BSC	
L	0.30	0.35	0.40
k	0.20	--	--

Tape Information

DNF6 (2mm × 2mm)



Marking Information



X = Output Version

61XXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2023-09-15	Preliminary Version	Tu guozhu	Gu jie, Liu xiaomin	Liu jiaying
0.1	2025-04-21	Official Version	Peng junjie	Gu jie, Liu xiaomin	Liu jiaying
1.1	2025-06-04	Update DFN6 Package	Peng junjie	Gu jie, Liu xiaomin	Liu jiaying
1.2	2025-09-08	Update EC table	Peng junjie	Gu jie, Liu xiaomin	Liu jiaying