

CE5HL5XXC1Q - High Input Very-Low I_Q 300mA LDO

General Description

CE5HL5XXC1Q is the high input very low I_Q 300mA LDO with enable function that operates from 1.8V~12V, is designed specifically for portable battery-powered applications which require ultra-low quiescent current. The very-low consumption of type 2.8μA ensures long battery life and dynamic transient boost feature improves device transient response for wireless communication applications.

CE5HL5XXC1Q offered SOT89-5 package and operates over an ambient temperature range of -40°C to 125°C.

Features

- Wide Input Voltage Range from 3.0V to 40V
- Up to 300mA Load Current
- Very Low I_Q is 2.8μA Typical
- Fixed Output Voltage are 1.8V, 3.0V, 3.3V, 3.6V, 5.0V, 6.0V, 7.0V, 8.0V, 9.0V, 12V, etc.
- Low Dropout is 900mV at 300mA Load @V_{OUT} = 5.0V
- Excellent Load/Line Transient Response
- High Ripple Rejection: 52dB at 1KHz
- Automotive AEC-Q100 Grade 1 Qualified
 - Ambient Temperature Range of -40°C to 125°C
 - ESD HBM 2KV PASS
 - ESD CDM 1.5KV PASS
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
CE5HL5XXC1Q	SOT89-5	Tape and Reel, 1K/Reel	1

Device information

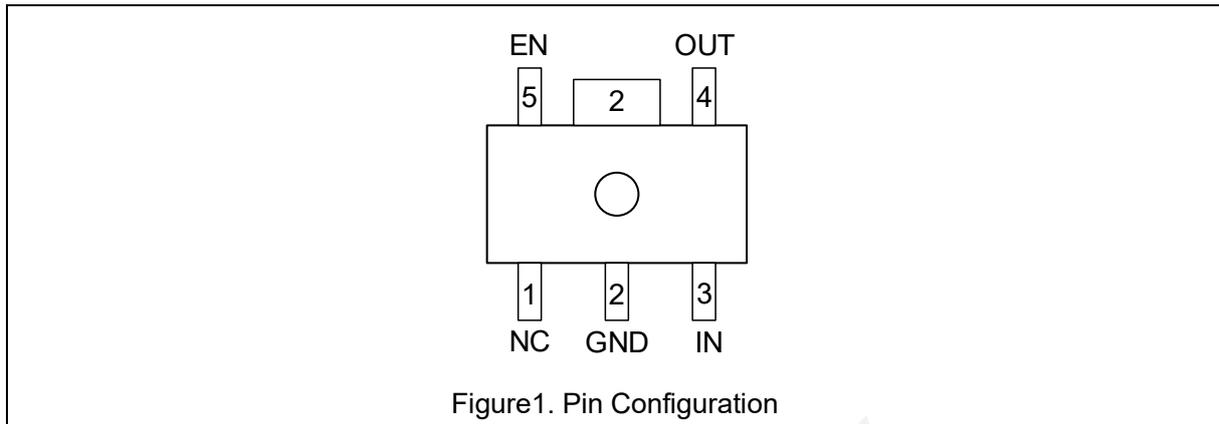
CE5HL5 XX C1 Q

<u>XX</u>	Output Voltage	<u>C1</u>	Package	<u>Q</u>	AEC-Q100 Qualified
XX	X.XV Output Voltage For example, 33 is 3.3V output	C1	SOT89-5	Q	With AEC-Q100 Qualified

Application

- Automotive Device Power Supply
- Automotive Infotainment and Cluster

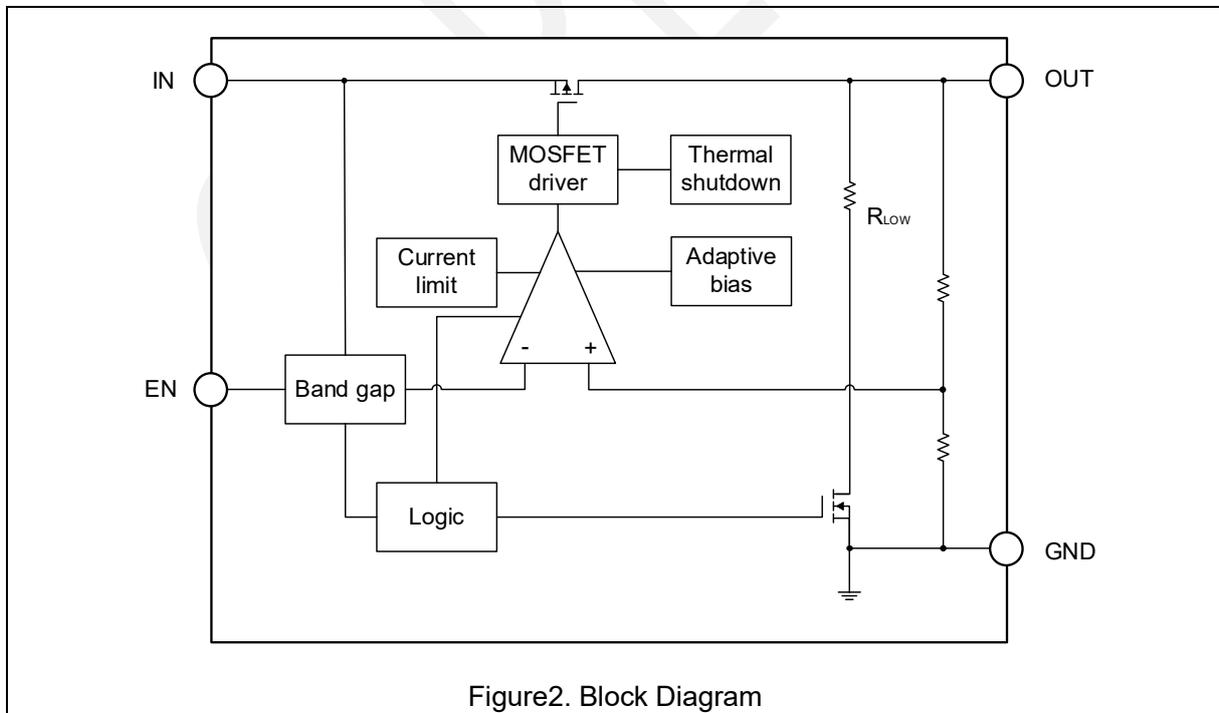
Pin Configuration



Pin Function

Pin No.	Pin Name	Pin Function
1	NC	No Connection.
2	GND	Ground Pin.
3	IN	Supply Input Pin.
4	OUT	Output Pin.
5	EN	Enable Control Input, Active High.

Block Diagram



Functional Description

Input Capacitor

A 1 μ F~10 μ F ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μ F to 10 μ F, Equivalent Series Resistance (ESR) is from 5m Ω to 100m Ω , and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Enable

The CE5HL5XXC1Q delivers output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Dropout Voltage

The CE5HL5XXC1Q uses a PMOS pass transistor to achieve low dropout. When ($V_{IN} - V_{OUT}$) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as ($V_{IN} - V_{OUT}$) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the ($V_{IN} - V_{OUT}$) voltage and the load current. For reliable operation, limit junction temperature to 150°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance. The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA} .

Current-Limit Protection

The CE5HL5XXC1Q provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

Absolute Maximum Ratings

Symbol	Rating		Value	Unit
$V_{IN}^{(1)}$	Input Voltage		-0.3~50	V
V_{OUT}	Output Voltage		-0.3~15	V
V_{EN}	Chip Enable Input		-0.3~50	V
$T_{J(MAX)}$	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65~150	°C
$V_{ESD}^{(2)}$	ESD Classification	Human Body Model	2000	V
		Charged Device Model	1500	V
$L_U^{(2)}$	Latch Up Current Maximum Rating		200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: Refer to Electrical Characteristics and Application Information for Safe Operating Area.

Note2: This device series incorporates ESD protection and is tested by the following methods:

HBM tested per AEC-Q100-002(JEDEC JS-001);

CDM tested per AEC-Q100-011(JEDEC JS-002);

Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Thermal Characteristics

Symbol	Package	Ratings	Value	Unit
$R_{\theta JA}$	SOT89-5	Thermal Characteristics, Thermal Resistance, Junction-to-Air	80	°C/W
Power Dissipation	SOT89-5	PCB Board Dimension: 40mm x 40mm (2layer) Copper :1OZ @25°C	1500	mW

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	3.0 to 40	V
I_{OUT}	Output Current	0 to 300	mA
T_A	Operating Ambient Temperature	-40 to 125	°C
C_{IN}	Effective Input Ceramic Capacitor Value	1 to 10	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance (ESR)	5 to 100	mΩ

Electrical Characteristics

($V_{IN} = V_{OUT} + 2V$; $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 1\mu F$, $T_A = -40^{\circ}C \sim 125^{\circ}C$ unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage ⁽³⁾		3.0		40	V
V_{OUT}	Output Voltage	$I_{OUT} = 1mA$, $T_A = 25^{\circ}C$	-1.5%		1.5%	V
		$I_{OUT} = 1mA$, $T_A = -40 \sim 125^{\circ}C$	-2%		2%	
I_Q	Quiescent Current	$I_{OUT} = 0mA$, $T_A = 25^{\circ}C$		2.8	6.5	μA
I_{Q_OFF}	Standby Current	$V_{EN} = 0V$, $T_A = 25^{\circ}C$			1	μA
Line _{REG}	Line Regulation ⁽⁶⁾	$V_{IN} = V_{OUT} + 2V$ to 40V, $I_{OUT} = 10mA$		40	90	mV
Load _{REG}	Load Regulation ⁽⁶⁾	$1mA \leq I_{OUT} \leq 300mA$, $V_{IN} = V_{OUT} + 2V$		90	180	mV
V_{DROP}	Dropout Voltage $I_{OUT} = 300mA$ ⁽⁴⁾ ⁽⁶⁾	$V_{OUT} = 1.8V$		950	1450	mV
		$V_{OUT} = 3.0 \sim 13V$		1000	1500	
I_{LMT}	Current Limit	$V_{IN} = V_{OUT} + 2V$		450	800	mA
I_{SHORT}	Short Current Limit	$V_{OUT} = 0V$		55	120	mA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage "H"	1.4			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage "L"			0.4	V
I_{EN}	EN Pin Current	$V_{EN} = 0 \sim 40V$		1		μA
PSRR ⁽⁵⁾	Power Supply Rejection Ratio	$f = 1kHz$, $V_{IN} = V_{OUT} + 2V$ $I_{OUT} = 20mA$		52		dB
e_N ⁽⁵⁾	Output Noise Voltage	$V_{IN} = V_{OUT} + 2V$, $I_{OUT} = 1mA$, $f = 10Hz$ to 100KHz, $V_{OUT} = 3V$, $C_{OUT} = 1\mu F$		30* V_{OUT}		μV_{rms}
T_{ON}	Turn-On Time	From Assertion of V_{EN} to $V_{OUT} = 90\%V_{OUT(NOM)}$		1		ms
T_{TSD} ⁽⁵⁾	Thermal Shutdown Temperature	Temperature Increasing from $T_A = 25^{\circ}C$		155		$^{\circ}C$
T_{HYS} ⁽⁵⁾	Thermal Shutdown Hysteresis	Temperature Falling from T_{TSD}		25		$^{\circ}C$

Note3: Here V_{IN} means internal circuit can work normal. If $V_{IN} < V_{OUT}$, Output voltage follows $V_{IN}(I_{OUT} = 1mA)$, circuit is safety.

Note4: V_{DROP} FT test method: test the V_{OUT} voltage at $V_{OUT} + V_{DROPMAX}$ with 300mA output current.

Note5: Guaranteed by design and characterization. not a FT item.

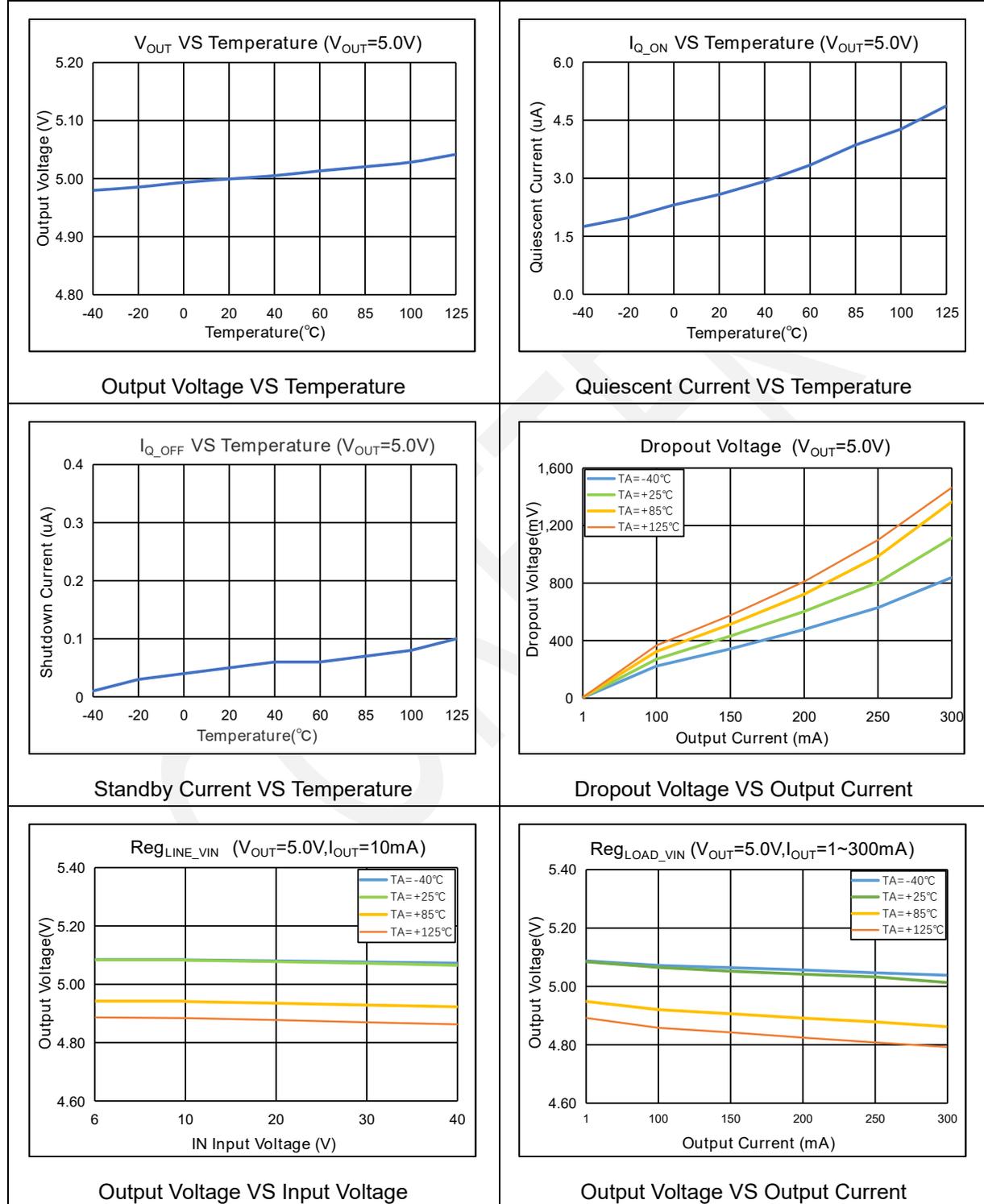
Note6: At high temperatures, the maximum load current can be calculated according to the following formula:

$$I_{OUT_MAX} = (T_J - T_A) / R_{\theta JA} / (V_{IN} - V_{OUT})$$

Typical Characteristics

V_{OUT} = 5.0V Version

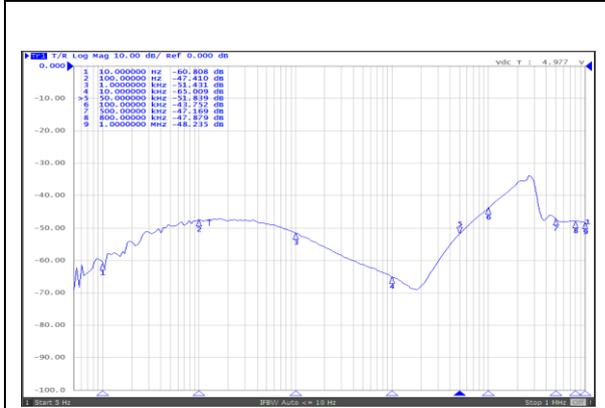
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



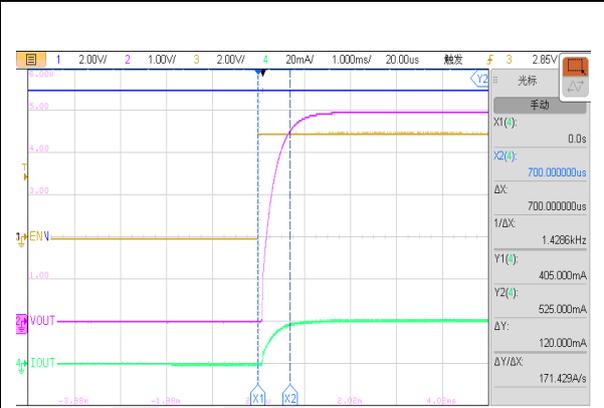
Typical Characteristics (Continued)

V_{OUT} = 5.0V Version

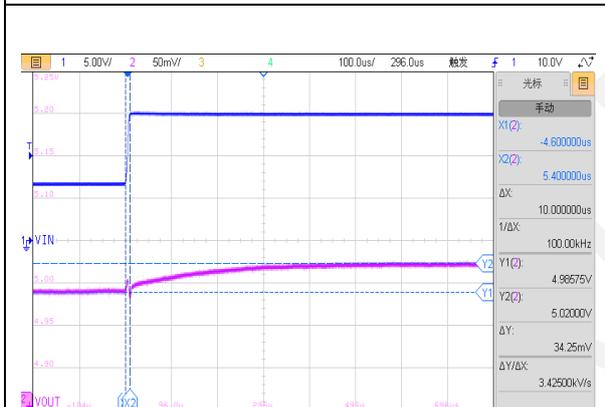
((V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



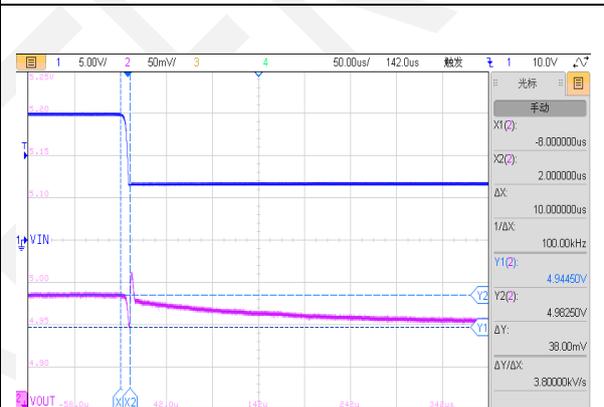
PSRR (I_{OUT} = 20mA)



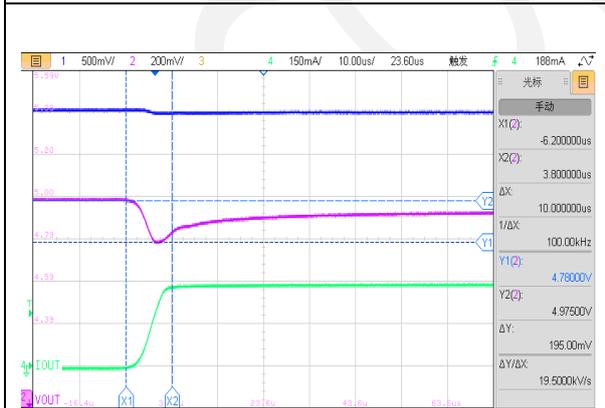
T_{ON} (I_{OUT} = 20mA)



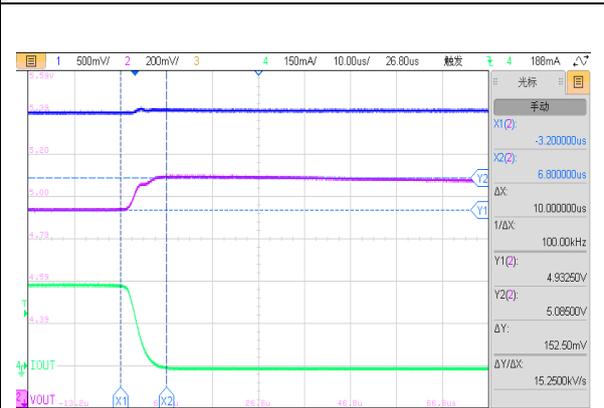
Input-Transient (7~15V, t_r = 10μs, I_{OUT} = 1mA)



Input-Transient (15~7V, t_r = 10μs, I_{OUT} = 1mA)

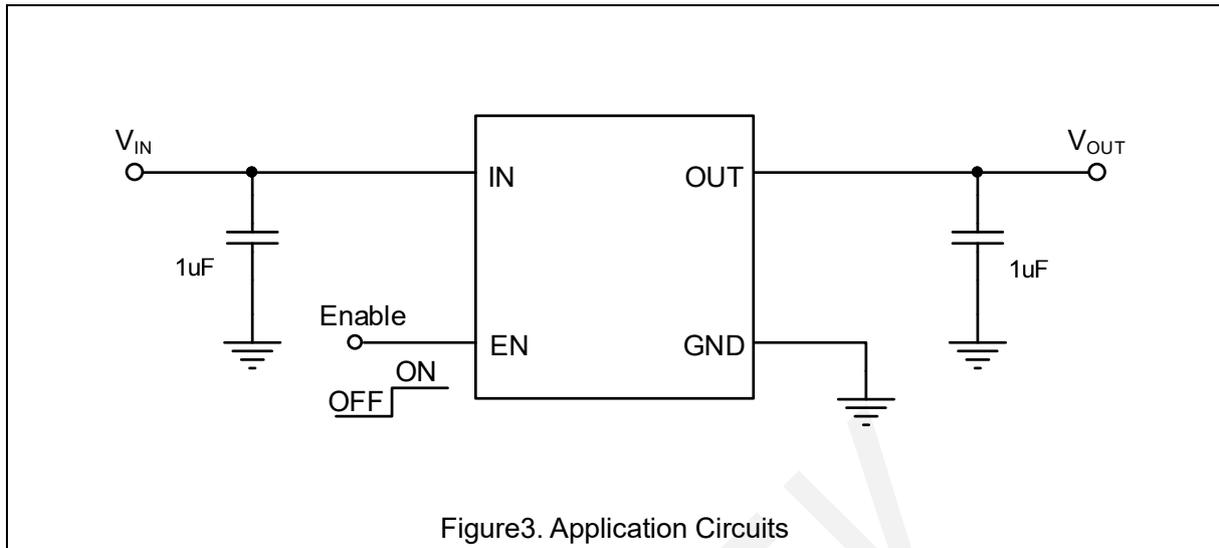


Load-Transient (V_{IN} = 7.0V, I_{OUT} = 1~300mA, t_r = 10μs)



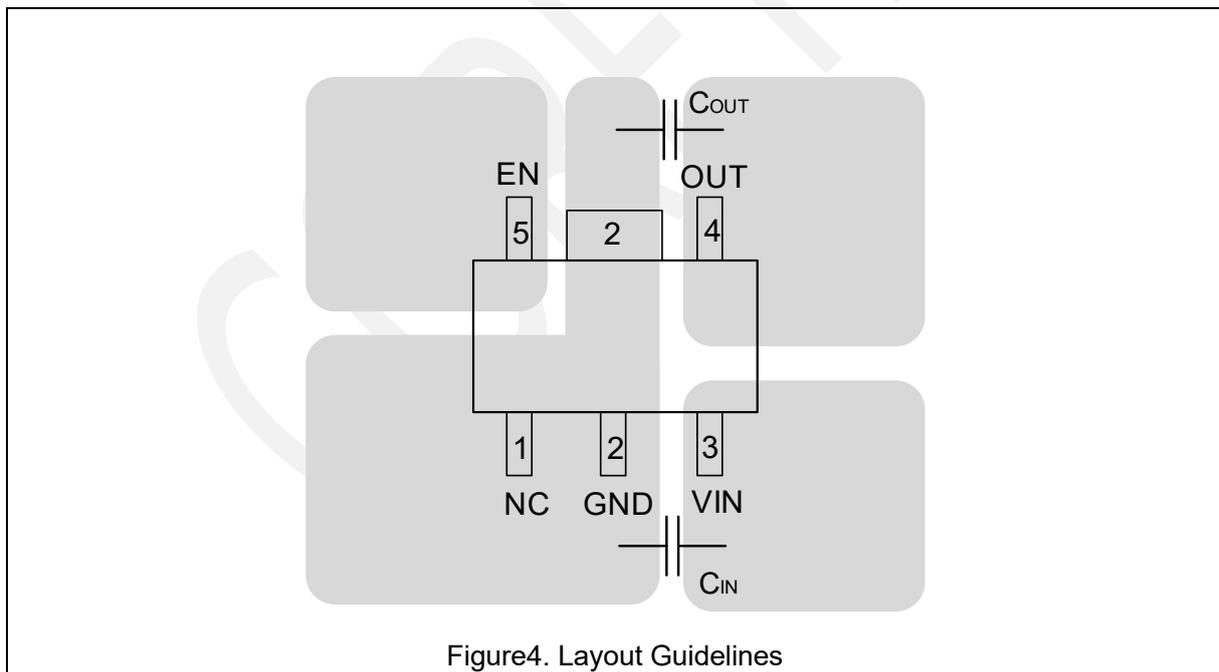
Load-Transient (V_{IN} = 7.0V, I_{OUT} = 300~1mA, t_r = 10μs)

Application Circuits



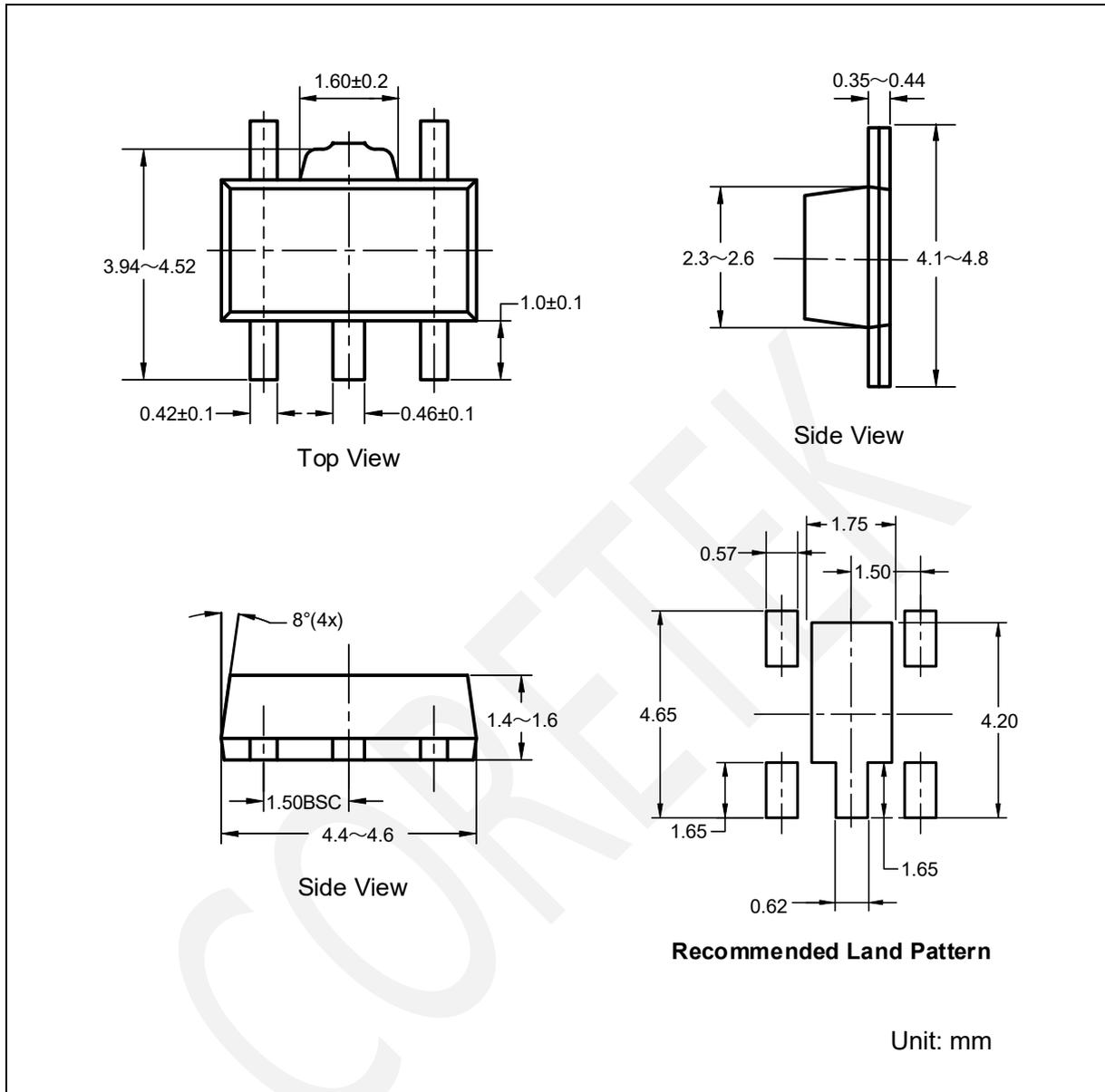
Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.

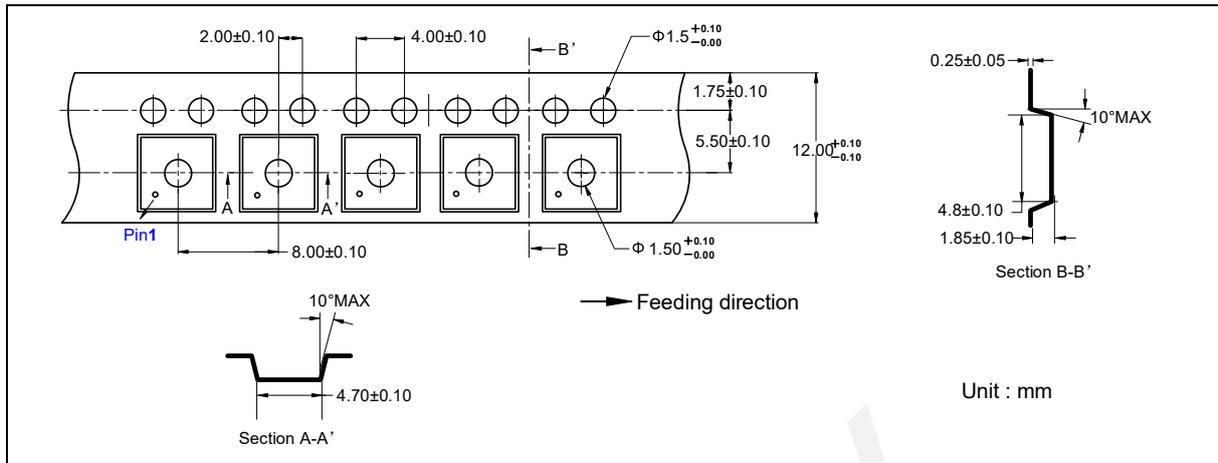


Package Dimension

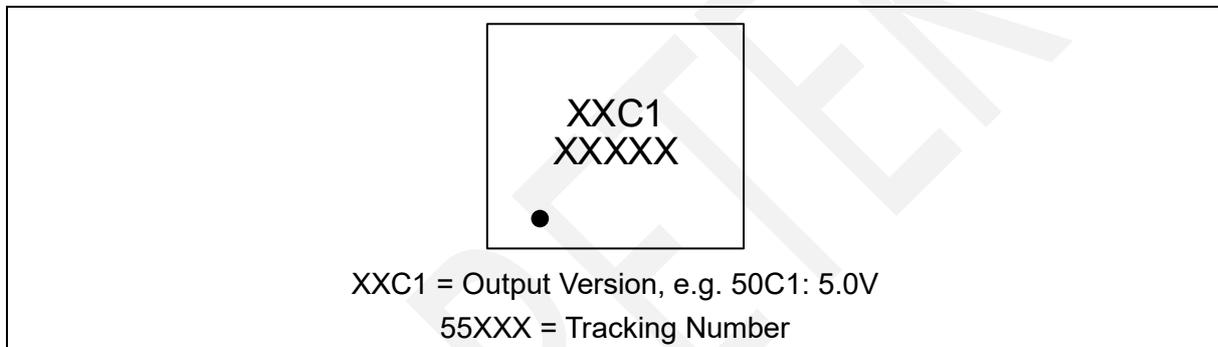
SOT89-5



Tape Information



Marking Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2022-11-13	Preliminary Version	Liu xiaomin	Liu xiaomin	Zhu junli
0.1	2023-07-21	AEC-Q100 version	Shi bo	Liu xiaomin	Zhu junli
0.2	2024-12-10	Update Pin Configuration	Peng junjie	Liu xiaomin	Zhu junli
1.0	2025-02-10	Official Version	Peng junjie	Liu xiaomin	Zhu junli
1.0.a	2025-09-10	Update AEC-Q100 Grade	Peng junjie	Liu xiaomin	Zhu junli