

CE5HL2XXQ - High Input Very-Low IQ 300mA LDO

General Description

CE5HL2XXQ is the high input very low IQ 300mA LDO with enable function, is designed specifically for automotive applications. There have very-low power consumption of type 2.5 μ A and dynamic transient boost feature improves device transient response.

CE5HL2XXQ offered SOT23-5 package and operates ambient temperature range of -40°C to 125°C.

Features

- Wide Input Voltage Range from 2.8V to 36V
- Up to 300mA Load Current
- Very Low I_Q is 2.5 μ A Typical
- Fixed Output Voltage are 1.8V, 2.5V, 2.8V, 3.0V, 3.3V, 3.6V, 4.0V, 5.0V and etc
- Low Dropout is 1000mV at 300mA Load @ $V_{OUT} = 3.3V$
- Excellent Load/Line Transient Response
- High Ripple Rejection: 60dB at 1KHz
- Automotive AEC-Q100 Grade 1 Qualified
 - Ambient Temperature Range of -40°C to 125°C
 - ESD HBM 2KV PASS
 - ESD CDM 1.5KV PASS
- Latch-up Performance Exceeds $\pm 200mA$ per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
CE5HL2XXQ	SOT23-5 (1.6mm \times 2.9mm)	Tape and Reel, 3K/Reel	1

Device information

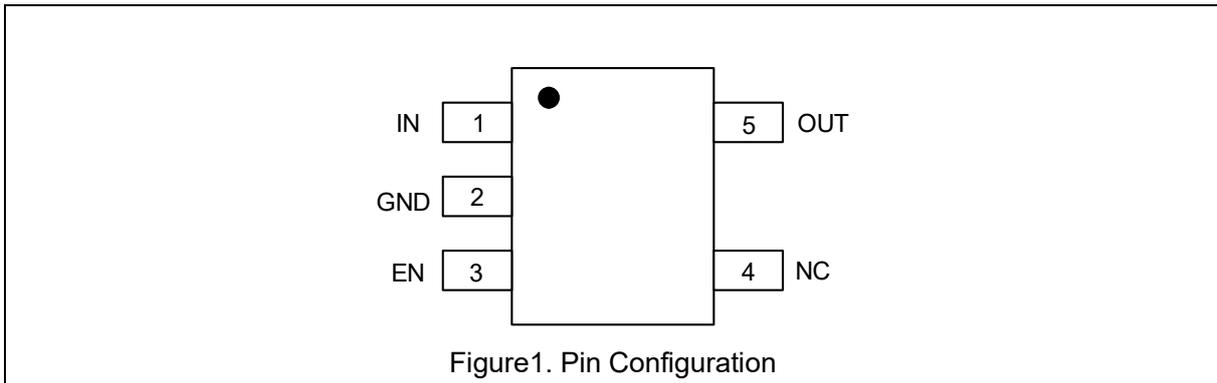
CE5HL2 XX Q

<u>XX</u> Output Voltage		<u>Q</u> AEC-Q100 Qualified	
XX	X.XV Output Voltage For example, 33 is 3.3V output	Q	With AEC-Q100 Qualified

Applications

- Automotive Constant-Voltage Power Supply
- Automotive Infotainment and Cluster
- Automotive Power Supply for Body Electronics and Lighting

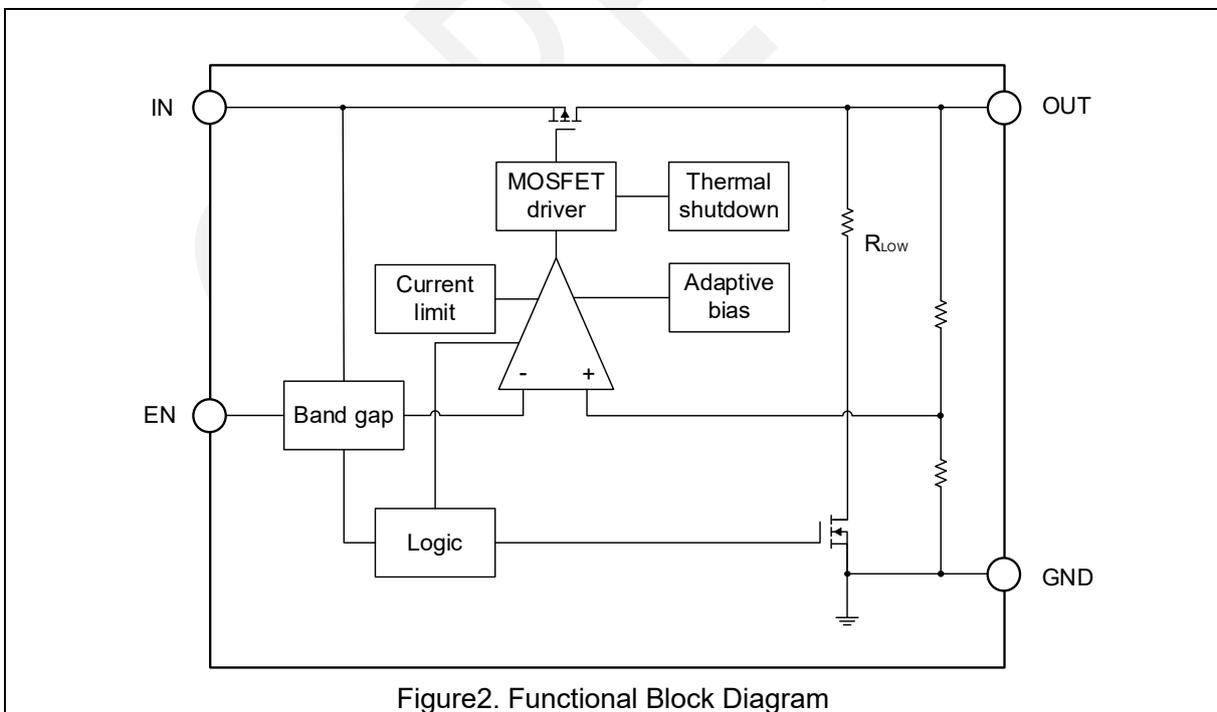
Pin Configuration



Pin Function

Pin No.	Pin Name	Pin Function
1	IN	Supply Input Pin
2	GND	Ground Pin
3	EN	Enable Input Pin, "H" Active
4	NC	No Connection
5	OUT	Output Pin

Block Diagram



Functional Description

Input Capacitor

A 1 μ F~10 μ F ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1 μ F to 10 μ F, Equivalent Series Resistance (ESR) is from 5m Ω to 100m Ω , and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Enable

The CE5HL2XXQ delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Dropout Voltage

The CE5HL2XXQ uses a PMOS pass transistor to achieve low dropout. When ($V_{IN} - V_{OUT}$) is less than the dropout voltage (VDO), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. VDO scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as ($V_{IN} - V_{OUT}$) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 125°C, the output circuitry is again enabled.

Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the ($V_{IN} - V_{OUT}$) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 150°C and T_A is the ambient temperature. The junction to ambient thermal resistance (θ_{JA}) is layout dependent.

Current-Limit Protection

The CE5HL2XXQ provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

Absolute Maximum Ratings

Symbol	Rating	Value	Unit	
V_{IN}	Input Voltage ⁽¹⁾	-0.3~44	V	
V_{OUT}	Output Voltage	-0.3~6	V	
V_{EN}	Chip Enable Input	-0.3~44	V	
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C	
T_{STG}	Storage Temperature	-65~150	°C	
V_{ESD} ⁽²⁾	ESD Classification	Human Body Model	±2000	V
		Charged Device Model	±1500	V
I_{LU} ⁽²⁾	Latch up Current Maximum Rating	±200	mA	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.

Note2. This device series incorporates ESD protection and is tested by the following methods:

HBM tested per AEC-Q100-002(JEDEC JS-001);

CDM tested per AEC-Q100-011(JEDEC JS-002);

Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Thermal Characteristics

Symbol	Ratings	Value	Unit
$R_{\theta JA}$	Thermal Characteristics, Thermal Resistance, Junction-to-Air	250	°C/W
P_D	Max Power Dissipation @25°C	0.5	W

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	2.8 to 36	V
I_{OUT}	Output Current	0 to 300	mA
T_A	Operating Ambient Temperature	-40 to 125	°C
C_{IN}	Effective Input Ceramic Capacitor Value	1 to 10	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	µF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

($V_{IN} = V_{OUT} + 2V$; $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 1\mu F$, $T_A = -40^{\circ}C \sim 125^{\circ}C$ unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage ⁽³⁾		2.8		36	V
V_{OUT}	Output Voltage	$I_{OUT} = 1mA$, $T_A = 25^{\circ}C$	-2%		2%	V
		$I_{OUT} = 1mA$, $T_A = -40\sim 125^{\circ}C$	-3%		3%	
I_Q	Quiescent Current	$I_{OUT} = 0mA$, $T_A = 25^{\circ}C$		2.5	4.5	μA
I_{Q_OFF}	Standby Current	$V_{EN} = 0V$, $T_A = 25^{\circ}C$		0.1	1	μA
$Line_{REG}$	Line Regulation ⁽⁶⁾	$V_{IN} = V_{OUT} + 2V$ to 36V, $I_{OUT} = 10mA$ ($\Delta V_{OUT} / \Delta V_{IN} / V_{OUT}$)		0.05	0.20	%/V
$Load_{REG}$	Load Regulation ⁽⁶⁾	$1mA \leq I_{OUT} \leq 300mA$, $V_{IN} = V_{OUT} + 2V$			40	mV
V_{DROP}	Dropout Voltage $I_{OUT}=300mA$ ⁽⁴⁾ ⁽⁶⁾	$V_{OUT} = 1.8V$		1350	1850	mV
		$V_{OUT} = 2.5V$		1150	1650	
		$V_{OUT} = 2.8V$		1100	1600	
		$V_{OUT} = 3.0V$		1050	1550	
		$V_{OUT} = 3.3V$		1000	1500	
		$V_{OUT} = 3.6V$		950	1450	
		$V_{OUT} = 5V$		900	1400	
I_{LMT}	Current Limit	$V_{IN} = V_{OUT} + 2V$, $R_{OUT} = 1\Omega$	350	450		mA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage "H"	1.2			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage "L"			0.4	V
I_{EN}	EN Pin Current	$V_{EN} = 0\sim 36V$		1		μA
PSRR	Power Supply Rejection Ratio ⁽⁵⁾	$f = 1kHz$, $V_{IN} = V_{OUT} + 2V$ $I_{OUT} = 20mA$		60		dB
e_n	Output Noise Voltage ⁽⁵⁾	$V_{IN} = V_{OUT} + 2V$, $I_{OUT} = 1mA$, $f = 10Hz$ to 100KHz, $V_{OUT} = 3.3V$, $C_{OUT} = 1\mu F$		100		μV_{rms}
T_{SD}	Thermal Shutdown Temperature ⁽⁵⁾	Temperature Increasing from $T_A = 25^{\circ}C$		155		$^{\circ}C$
T_{HYS}	Thermal Shutdown Hysteresis ⁽⁵⁾	Temperature Falling from TSD		30		$^{\circ}C$

Note3: Here V_{IN} means internal circuit can work normal. If $V_{IN} < V_{OUT}$, Output voltage follows $V_{IN}(I_{OUT} = 1mA)$, circuit is safety.

Note4: V_{DROP} FT test method: test the V_{OUT} voltage at $V_{SET} + V_{DROP_{MAX}}$ with 300mA output current.

Note5: Guaranteed by design and characterization. not a FT item.

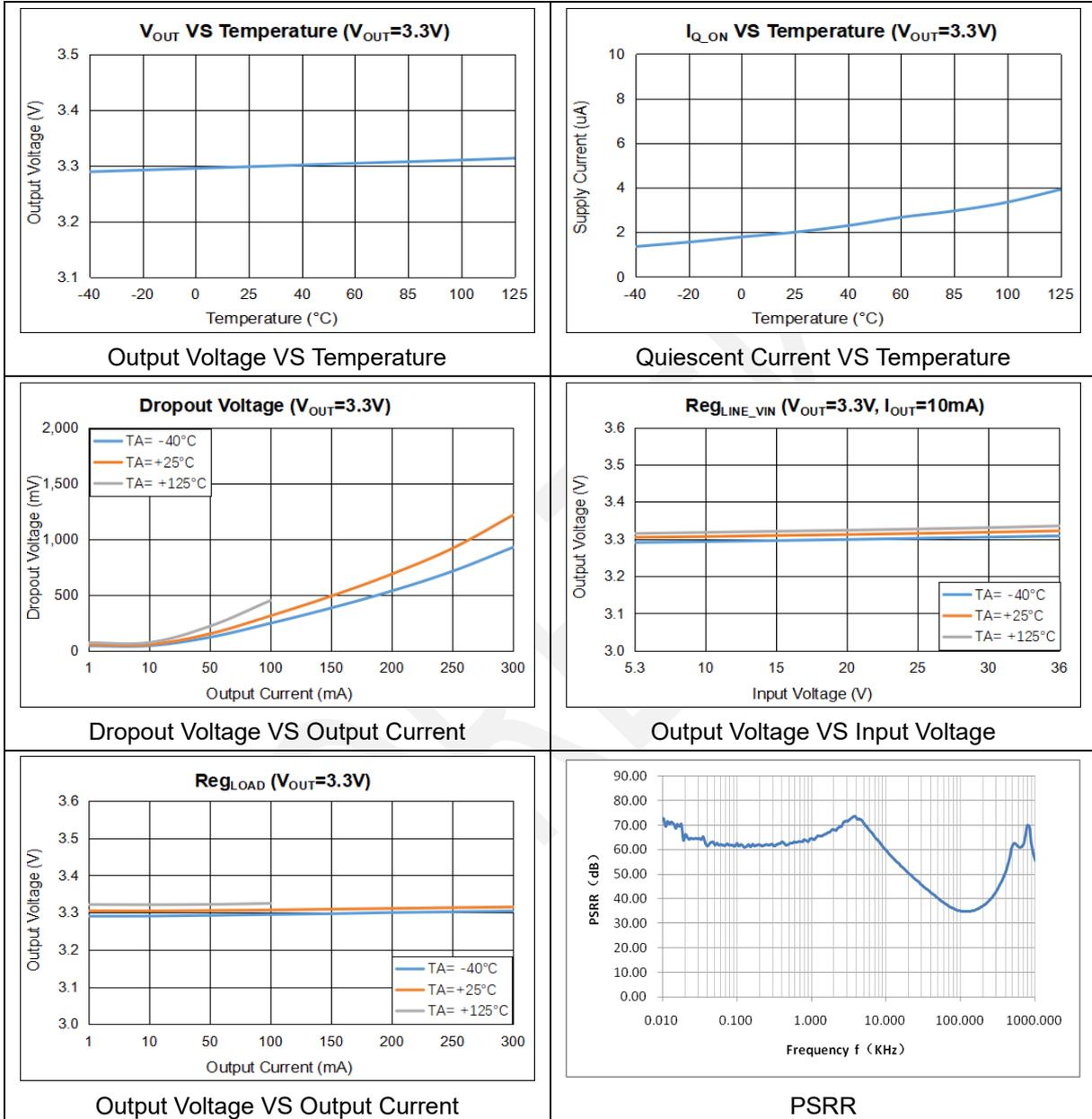
Note6: At high temperatures, the maximum load current can be calculated according to the following formula:

$$I_{OUT_MAX} = (T_J - T_A) / R_{\theta JA} / (V_{IN} - V_{OUT})$$

Typical Characteristics

VOLTAGE VERSION 3.3V

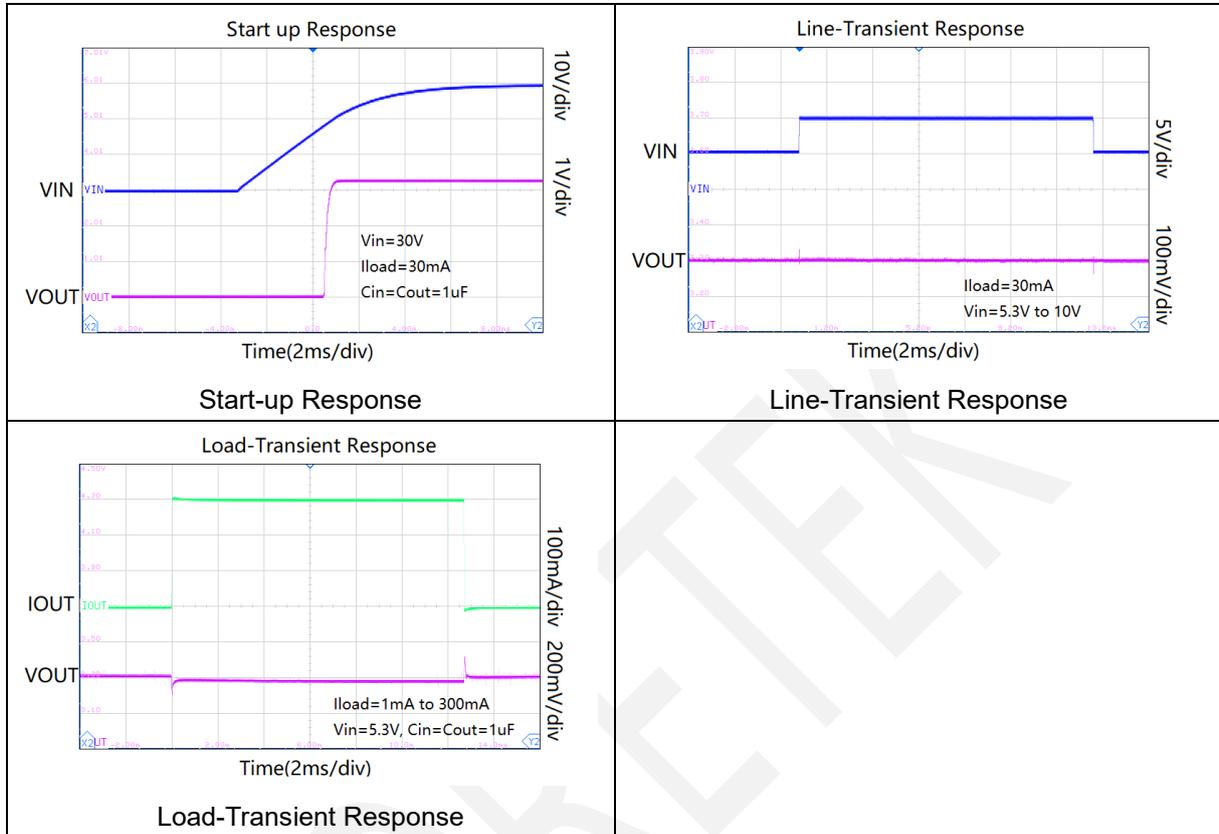
($V_{IN} = V_{OUT} + 2V$; $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 1\mu F$, $T_A = -40^{\circ}C \sim 125^{\circ}C$ unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)



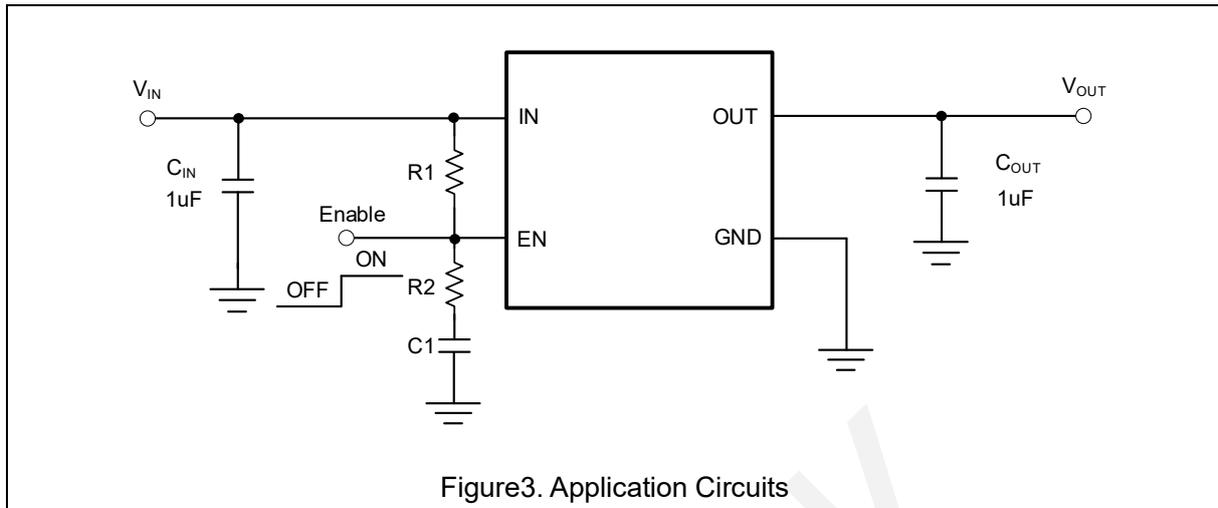
Typical Characteristics (Continued)

VOLTAGE VERSION 3.3V

($V_{IN} = V_{OUT} + 2V$; $I_{OUT} = 1mA$, $C_{IN} = C_{OUT} = 1\mu F$, $T_A = -40^{\circ}C \sim 125^{\circ}C$ unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)



Application Circuits

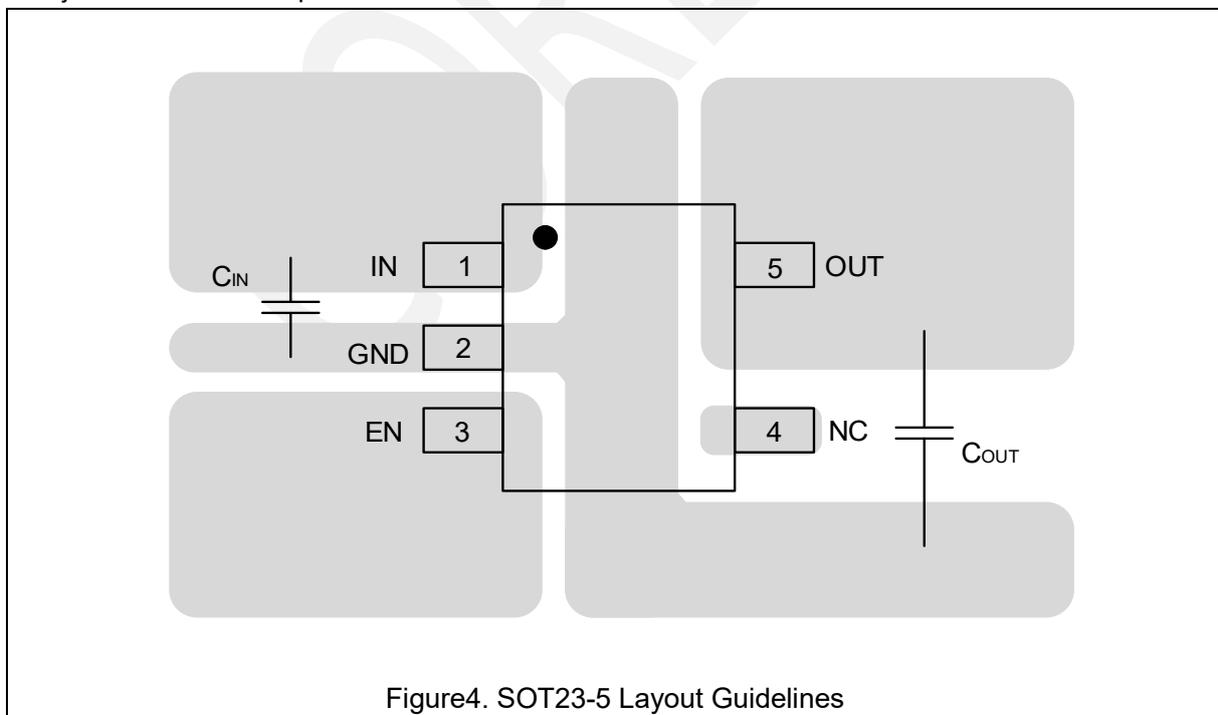


Note6: EN pin set resistor divider structure and Capacitor (for RC delay) is recommended.

$$V_{EN} = 2V \sim 6V, R1 = 10M\Omega, R2 = R1 / (V_{IN} / V_{EN} - 1), C1 = 4.7nF \sim 47nF.$$

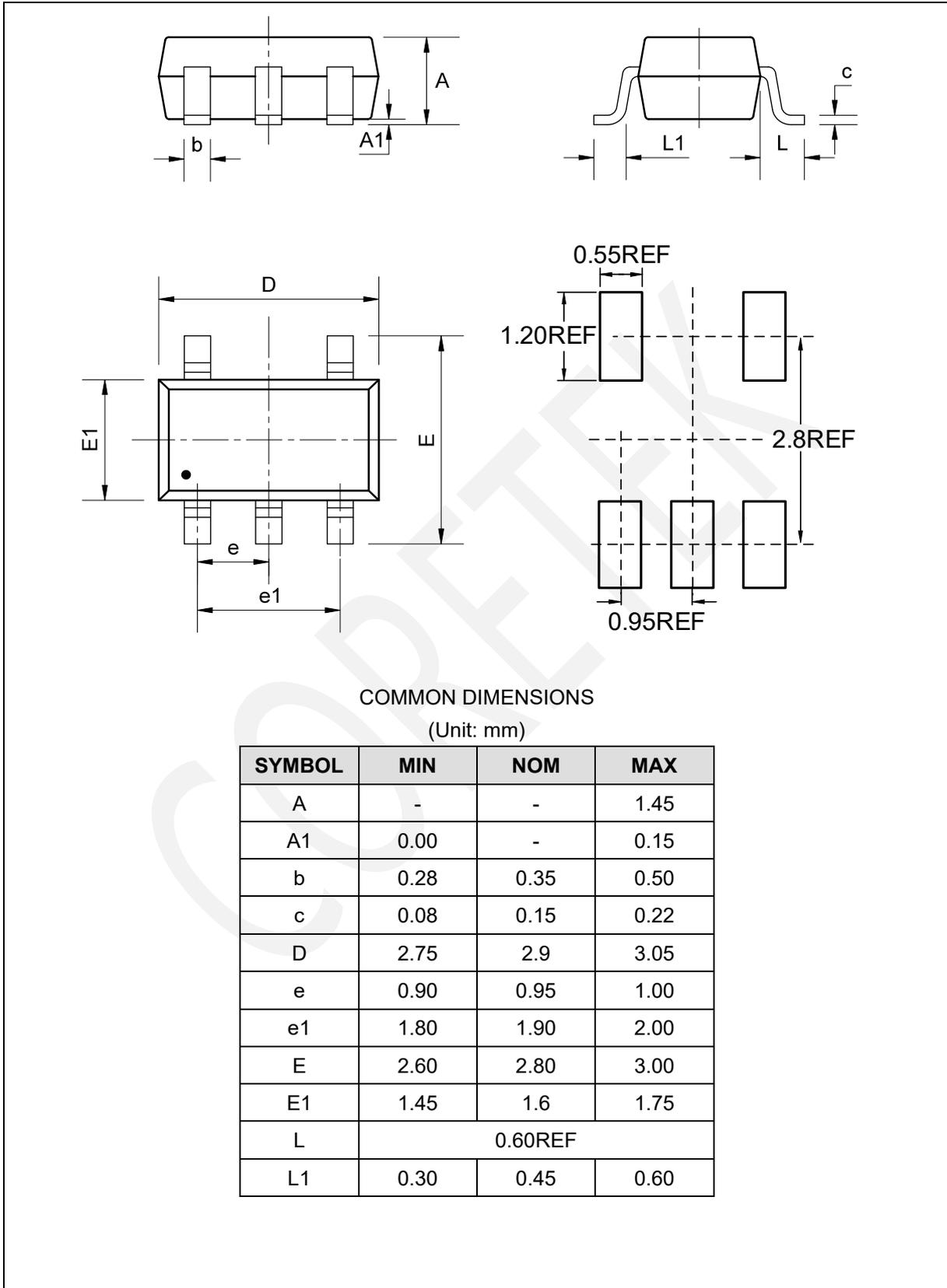
Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Do not place a thermal via directly beneath the thermal pad. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.



Package Dimension

SOT23-5 (1.6mm × 2.9mm)

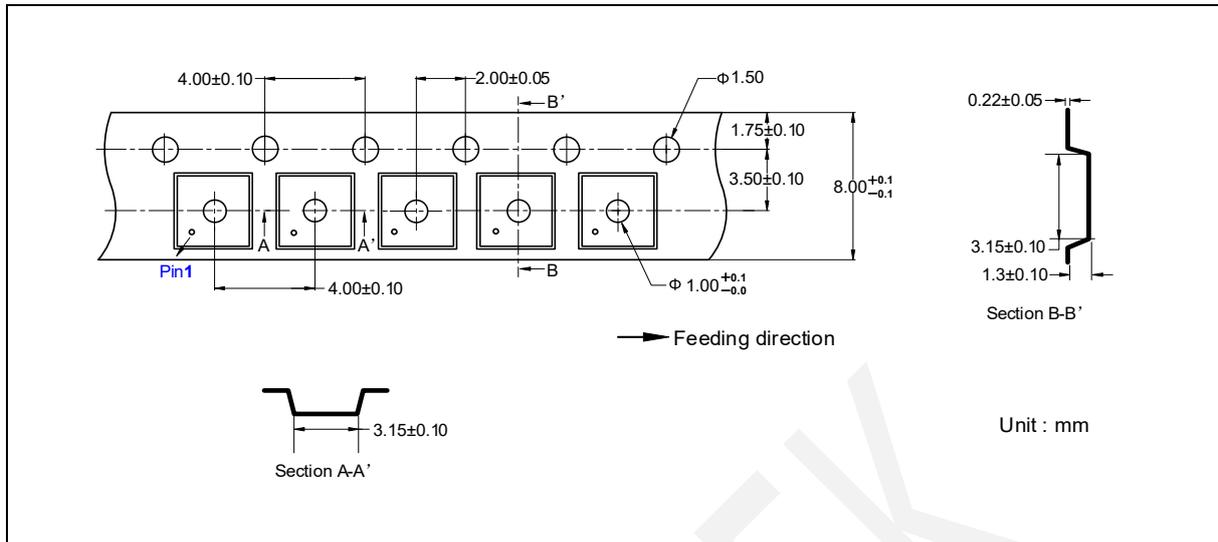


COMMON DIMENSIONS
(Unit: mm)

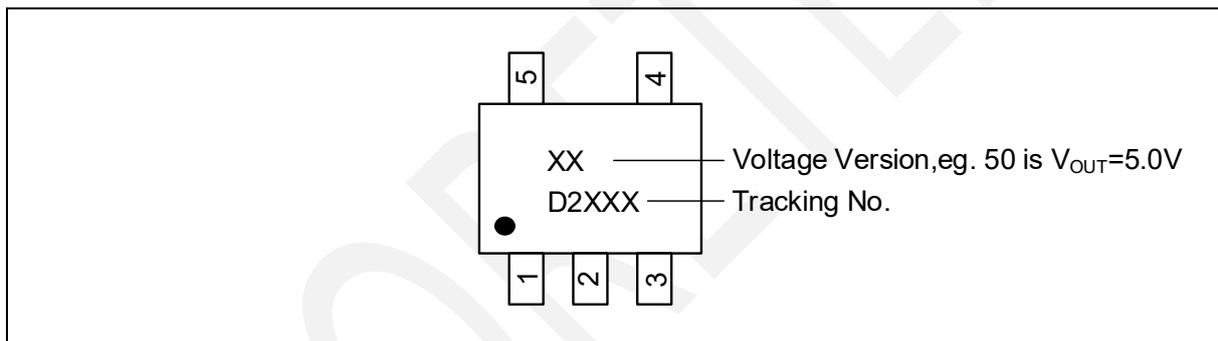
SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

Tape Information

SOT23-5 (1.6mm × 2.9mm)



Marking Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2019-10-22	Released Version	Liu xiaomin	Liu xiaomin	Zhu junli
1.1	2024-04-29	Update EC table	Yang xiaoxu	Liu xiaomin	Liu jiaying
1.2	2025-08-29	AEC-Q100 Version	Peng junjie	Liu xiaomin	Liu jiaying