CE5HL2XXM1Q - High Input 300mA LDO

General Description

CE5HL2XXM1Q is the high input very low I_Q LDO with enable function, is designed specifically for various automotive power supply. The very-low consumption of type 2.5μA ensures long power life and dynamic transient boost feature improves device transient response for automotive precision use applications.

CE5HL2XXM1Q offered ESOP8 package has good heat dissipation capability.

Features

- Wide Input Voltage Range from 2.5V to 36V
- Up to 300mA Load Current
- Very Low I_Q is 2.5μA Typical
- Fixed Output Voltage are 1.8V,2.5V,3.0V,3.3V,3.6V,5.0V,etc
- Low Dropout is 1000mV at 300mA Load @V_{OUT} = 3.3V
- Excellent Load/Line Transient Response
- High PSRR and Low Noise
- Good Heat Dissipation Performance
- Automotive AEC-Q100 Grade 1 Qualified
  -- Ambient Temperature Range of -40°C to 125°C
  -- ESD HBM 2KV PASS
  -- ESD CDM 1.5KV PASS
- Latch-up Performance Exceeds ±200mA per JEDEC JESD78F
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
CE5HL2XXM1Q	ESOP8 (4.9mm × 6.0mm)	Tape and Reel, 4K/Reel	3

Device information

CE 5HL2 XX M1 Q

XX Output Voltage		**M1** Package		**Q** AEC-Q100 Qualified
XX	X.XV Output Voltage For example, 33 is 3.3V output	M1	ESOP8	Q: With AEC-Q100 Qualified

Applications

- Automotive Constant-Voltage Power Supply
- Automotive Infotainment and Cluster
- Automotive Power Supply for Body Electronics and Lighting

Pin Configuration

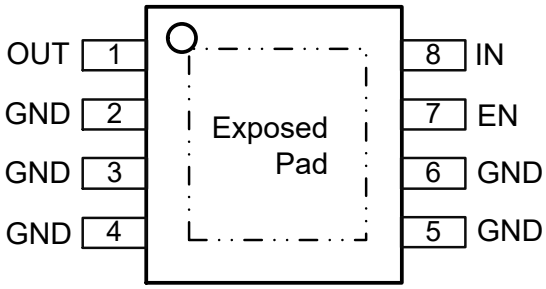


Figure1. Pin Configuration

Pin Function

Pin No.	Pin Name	Pin Function
1	OUT	Output Pin
2,3,4,5,6	GND	Ground Pin
7	EN	Enable Input Pin, “H” Active
8	VIN	Input Pin
	Exposed Pad	Thermal Pad, Recommend Floating or Connect to GND

Block Diagram

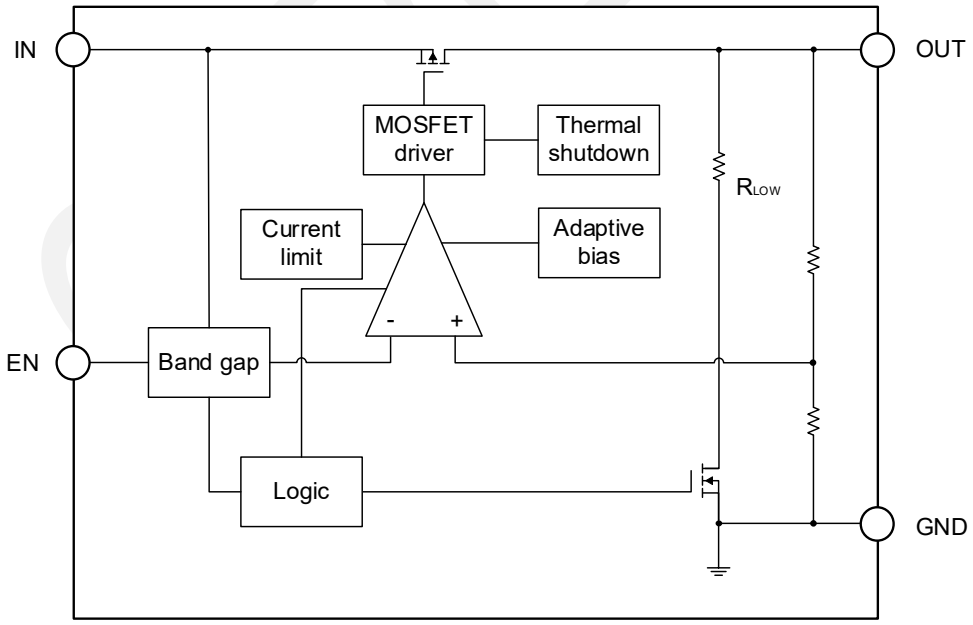


Figure2. Functional Block Diagram

Functional Description

Input Capacitor

A 1μF~10μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins.

Enable

The CE5HL2XXM1Q delivers the output power when it is set to enable state. When it works in disable state, there is no output power and the operation quiescent current is almost zero. The enable pin (EN) is active high.

Dropout Voltage

The CE5HL2XXM1Q uses a PMOS pass transistor to achieve low dropout. When (V_{IN} - V_{OUT}) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} - V_{OUT}) approaches dropout operation.

Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 155°C. Disabling the device eliminates the power dissipated by the device, allowing the device to cool. When the junction temperature cools to approximately 130°C, the output circuitry is again enabled.

Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the LDO from damage as a result of overheating. Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} - V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 150°C maximum.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 150°C and T_A is the ambient temperature. The junction to ambient thermal resistance θ_{JA} is layout dependent.

Current-Limit Protection

The CE5HL2XXM1Q provides current limit function to prevent the device from damages during over-load or shorted-circuit condition. This current is detected by an internal sensing transistor.

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{IN} (1)	Input Voltage	-0.3~44	V
V_{OUT}	Output Voltage	-0.3~6.0	V
V_{EN}	Chip Enable Input	-0.3~44	V
$T_{J(MAX)}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65~150	°C
V_{ESD} (2)	HBM Capability	±2000	V
	CDM Capability	±1500	V
I_{LU} (2)	Latch up Current Maximum Rating	±200	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Note1: Refer to Electrical Characteristics and Application Information for Safe Operating Area and IN port needs to be powered on before the EN port.

Note2: This device series incorporates ESD protection and is tested by the following methods:

HBM tested per AEC-Q100-002(JEDEC JS-001);

CDM tested per AEC-Q100-011(JEDEC JS-002);

Latch up Current Maximum Rating tested per AEC-Q100-004(JEDEC JESD78F).

Thermal Characteristics

Symbol	Ratings	Value	Unit
$R_{\theta JA}$	Thermal Characteristics, Thermal Resistance, Junction-to-Air	50	°C/W
P_D	Max Power Dissipation @25°C	2.5	W

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V_{IN}	Input Voltage	2.8 to 36	V
I_{OUT}	Output Current	0 to 300	mA
T_A	Operating Ambient Temperature	-40 to 125	°C
C_{IN}	Effective Input Ceramic Capacitor Value	1 to 10	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	1 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Operating Input Voltage (3)		2.8		36	V
V_{OUT}	Output Voltage	I_{OUT} = 1mA, T_A = 25°C	-2%		2%	V
		I_{OUT} = 1mA, T_A = -40~125°C	-3%		3%	
I_Q	Quiescent Current	I_{OUT} = 0mA, T_A = 25°C		2.5	6	μA
I_{Q_OFF}	Standby Current	V_{EN} = 0V, T_A = 25°C		0.1	3	μA
$Line_{REG}$	Line Regulation (6)	V_{IN} = V_{OUT} + 2V to 36V, I_{OUT} = 10mA (ΔV_{OUT} / ΔV_{IN} / V_{OUT})		0.05	0.20	%/V
$Load_{REG}$	Load Regulation (6)	1mA ≤ I_{OUT} ≤ 300mA, V_{IN} = V_{OUT} + 2V			40	mV
V_{DROP}	Dropout Voltage I_{OUT}=300mA (4) (6)	V_{OUT} = 1.8V		1350	1750	mV
		V_{OUT} = 2.5V		1150	1550	
		V_{OUT} = 2.8V		1100	1500	
		V_{OUT} = 3.0V		1050	1450	
		V_{OUT} = 3.3V		1000	1400	
		V_{OUT} = 3.6V		950	1350	
		V_{OUT} = 5.0V		900	1300	
I_{LMT}	Current Limit	V_{IN} = V_{OUT} + 2V, R_{OUT} = 1Ω	350	450		mA
V_{ENH}	EN Pin Threshold Voltage	EN Input Voltage “H”	1.2			V
V_{ENL}	EN Pin Threshold Voltage	EN Input Voltage “L”			0.4	V
I_{EN}	EN Pin Current	V_{EN} = 0~36V		1		μA
PSRR	Power Supply Rejection Ratio (5)	f = 1kHz, V_{IN} = V_{OUT} + 2V I_{OUT} = 20mA		60		dB
e_N	Output Noise Voltage (5)	V_{IN} = V_{OUT} + 2V, I_{OUT} = 1mA, f = 10Hz to 100KHz, V_{OUT} = 3.3V, C_{OUT} = 1μF		100		μVrms
T_{TSD}	Thermal Shutdown Temperature (5)	Temperature Increasing from T_A = 25°C		155		°C
T_{SDH}	Thermal Shutdown Hysteresis (5)	Temperature Falling from T_{TSD}		20		°C

Note3: Here V_{IN} means internal circuit can work normal. If V_{IN} < V_{OUT}, Output voltage follows V_{IN}(I_{OUT} = 1mA), circuit is safety.

Note4: V_{DROP} FT test method: test the V_{OUT} voltage at V_{OUT} + $V_{DROPMAX}$ with 300mA output current.

Note5: Guaranteed by design and characterization. not a FT item.

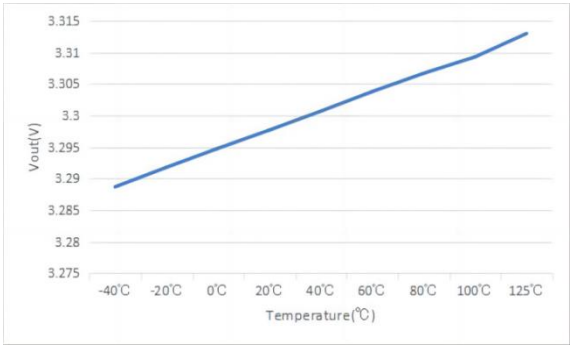
Note6: At high temperatures, the maximum load current can be calculated according to the following formula：

$$I_{OUT\_MAX} = (T_J - T_A) / R_{\theta JA} / (V_{IN} - V_{OUT})$$

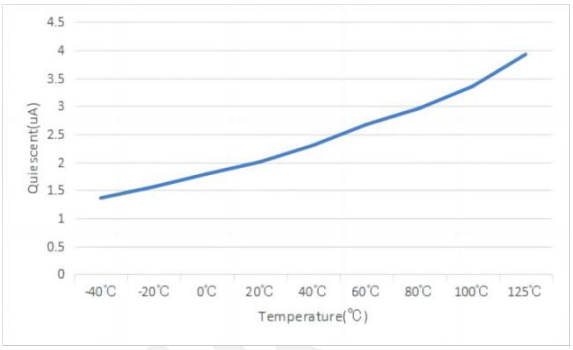
Typical Characteristics

VOLTAGE VERSION 3.3V

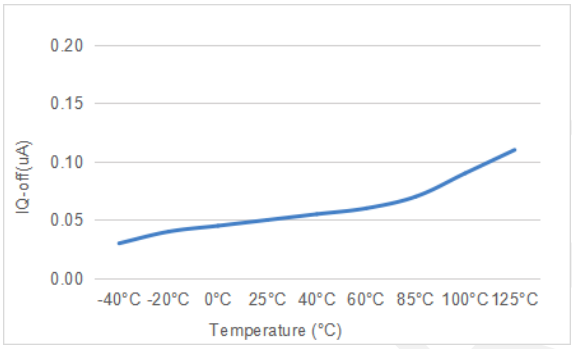
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



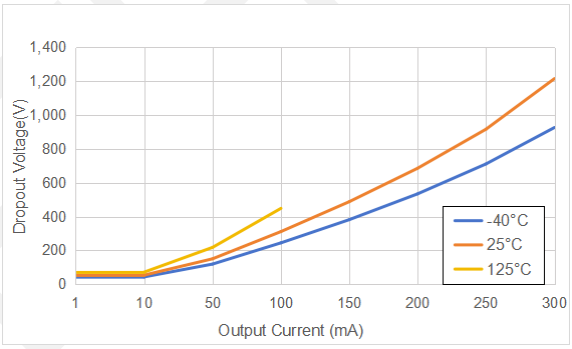
Output Voltage VS Temperature



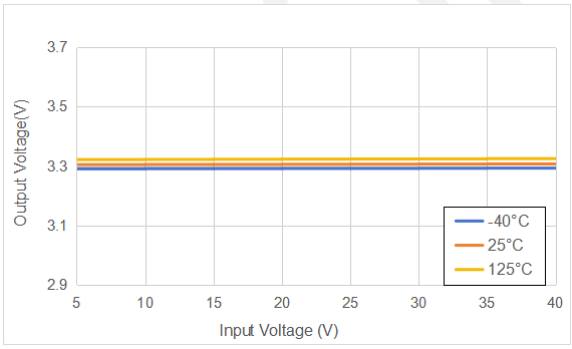
Supply Current VS Temperature



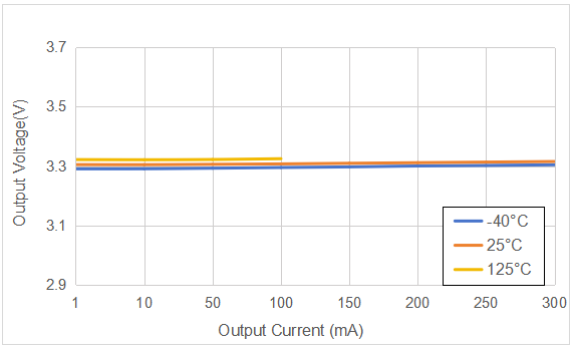
Standby Current VS Output Current



Dropout Voltage VS Output Current



Output Voltage VS Input Voltage

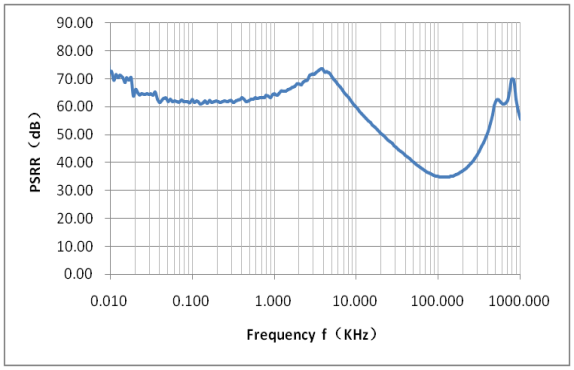


Output Voltage VS Output Current

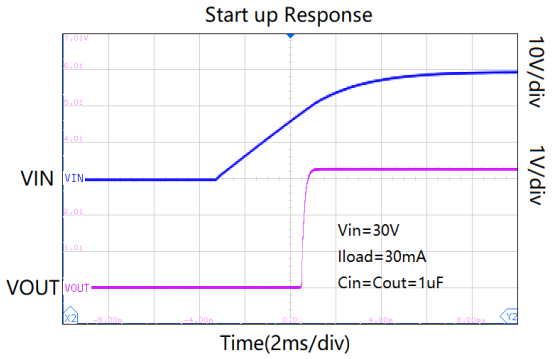
Typical Characteristics(Continued)

VOLTAGE VERSION 3.3V

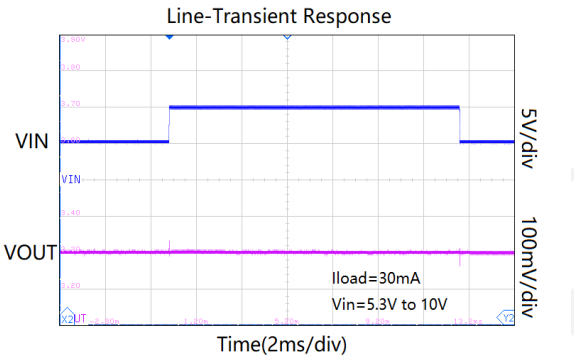
(V_{IN} = V_{OUT} + 2V; I_{OUT} = 1mA, C_{IN} = C_{OUT} = 1μF, T_A = -40°C~125°C unless otherwise noted. Typical values are at T_A = 25°C.)



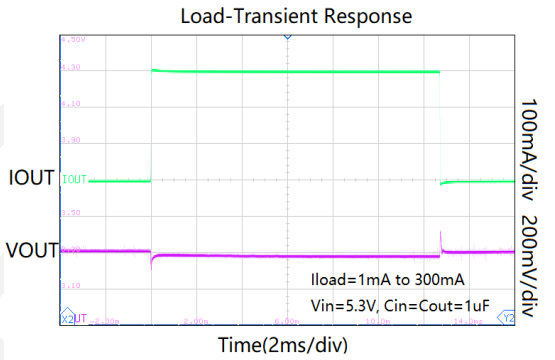
PSRR



Start-up Response



Line-Transient Response



Load-Transient Response

Application Circuits

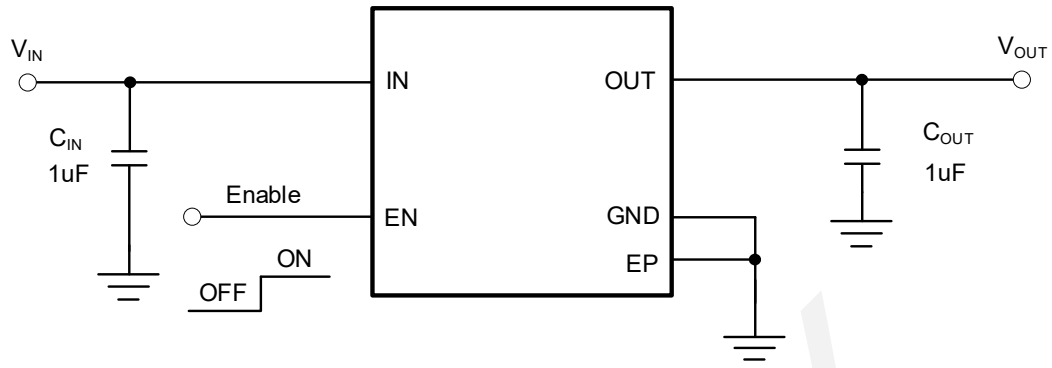


Figure3. Typical Application Circuit

Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections in order to optimize thermal performance.
- Place thermal vias around the device to distribute heat.
- Do not place a thermal via directly beneath the thermal pad. A via can wick solder or solder paste away from the thermal pad joint during the soldering process, leading to a compromised solder joint on the thermal pad.

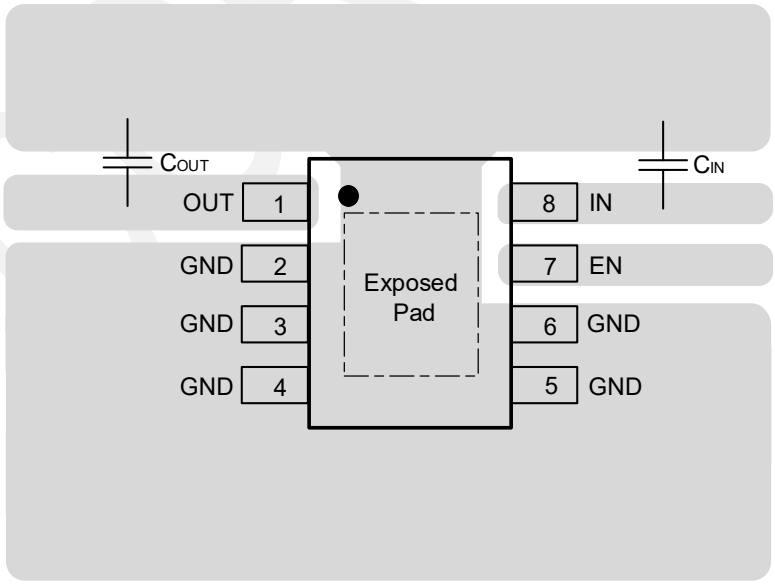
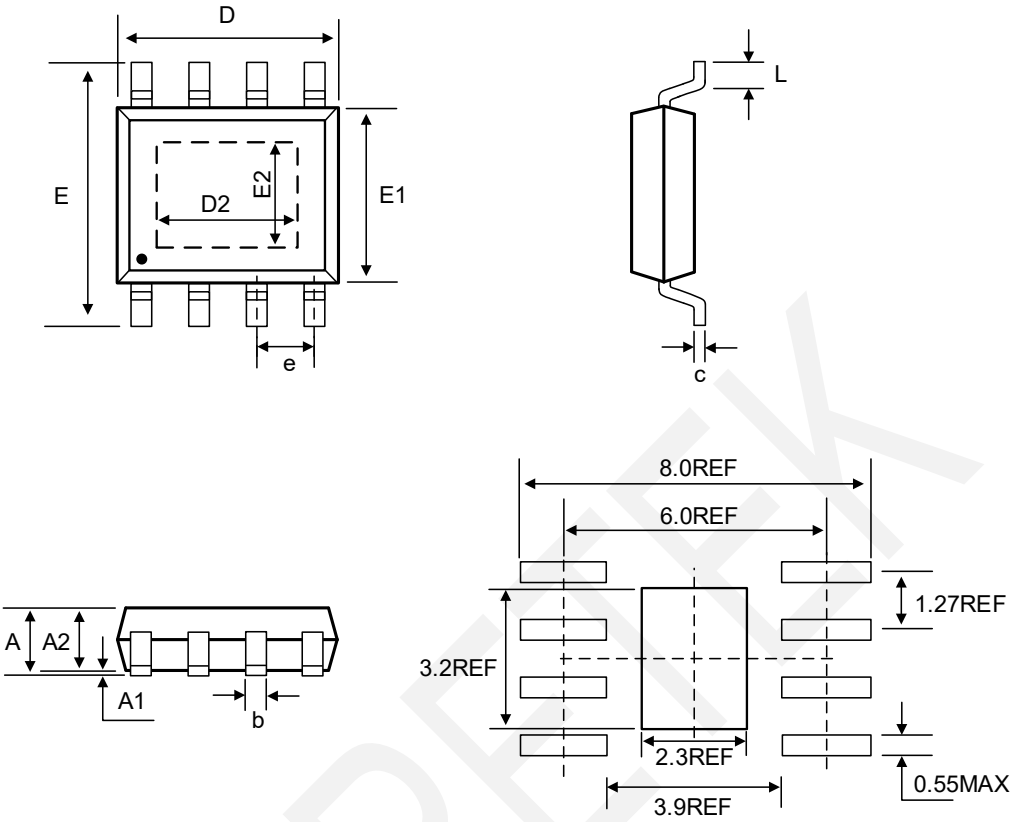


Figure4. Layout Guidelines

Package Dimension

ESOP8



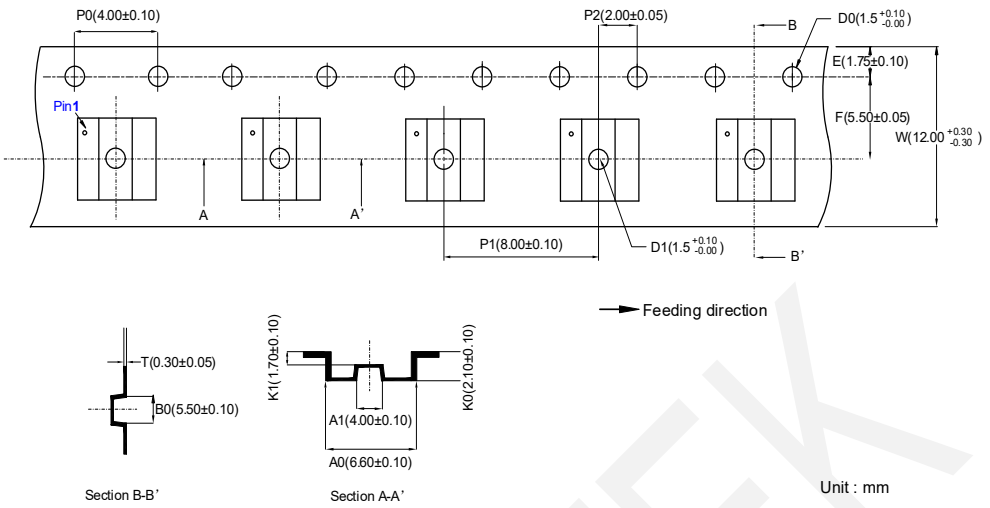
COMMON DIMENSIONS

(Unit: mm)

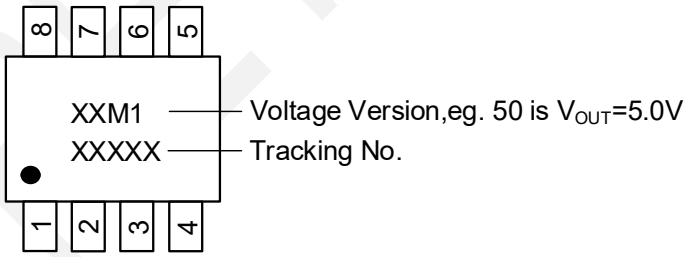
SYMBOL	MIN	NOM	MAX
A	-	-	1.90
A1	0.00	-	0.30
A2	1.20	1.40	1.60
b	0.35	-	0.51
c	0.15	-	0.27
D	4.70	4.90	5.10
E	5.80	6.00	6.20
D2	3.00	3.25	3.50
E1	3.70	3.90	4.10
E2	2.10	2.30	2.50
e	1.27BSC		
L	0.35	0.60	0.85

Tape Dimension

ESOP8



Marking Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2025-09-11	Official Version	Peng junjie	Gu jie,Liu xiaomin	Liu jiaying