CE53L8XX - 400mA Ultra-Low Noise, High PSRR LDO

General Description

The CE53L8XX of low-dropout (LDO), low-power linear regulators offer up to 400mA with PMOS pass transistor. The device offers low noise, high PSRR, low quiescent current and very good line/load transients, suitable for RF applications and analog circuits.

The CE53L8XX is stable with a 1μF input and 1uF ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve accuracy of 1.5%.

It is in a small SOT23-5 and DFN4 package, which is ideal for small form factor portable equipment such as wireless handsets.

Features

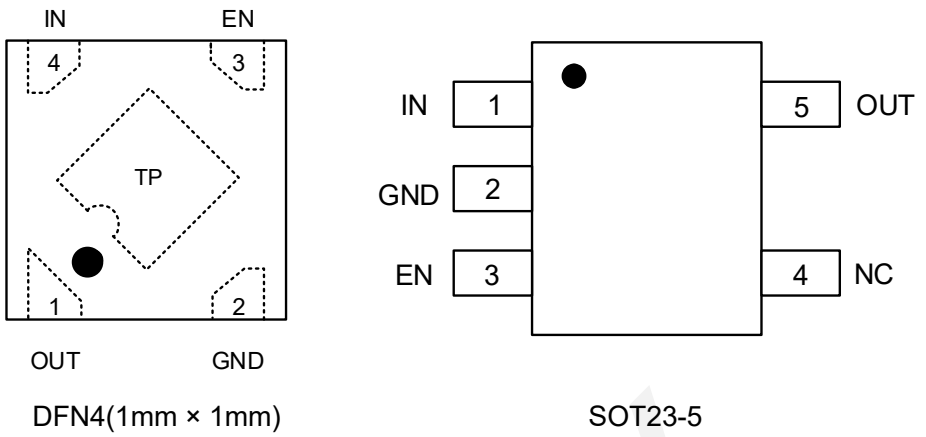
- Wide Input Voltage Range from 2.2V~5.5V
- Fixed Voltage: 3.3V, 3.6V
- Output Voltage Accuracy are ±1.5%
- Output Current are Up to 400mA
- Very Low I_Q of 20μA Typical
- Shutdown Current of 0.1uA Typical
- Low Dropout are Typical 150mV at 400mA, 3.3V Output
- Ultra Low Noise are Typical 8μV_{RMS} (Load = 200mA)
- Very High PSRR are 100dB at 1KHz, 45dB at 1MHz, 30mA
- Excellent Line/Load Transient Response
- With I_{LIMIT} Protection and Thermal Shutdown Circuit
- With Auto Discharge Function
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
CE53L8XXYB	DFN4 (1mm × 1mm)	Tape and Reel, 10K/Reel	1
CE53L8XX	SOT23-5 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3

Applications

- Smart Phones and Cellular Phones
- PDAs
- Digital Still Cameras
- Portable Instrument

Pin Configuration



DFN4(1mm × 1mm) SOT23-5

Figure1. Pin Configuration

Pin Function

Pin No.		Pin Name	Pin Function
DFN4	SOT23-5		
1	5	OUT	Output Pin. A 1μF low-ESR capacitor should be connected to this pin to ground.
2	2	GND	Ground
3	3	EN	Enable Control Input, active high. Do not leave EN floating
4	1	IN	Supply Input Pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor
TP		Thermal Pad	Thermal Pad for DFN4(1×1) Package, Connect to GND or Leave Floating. Do not connect to any potential other than GND.
	4	NC	No Connection.

Block Diagram

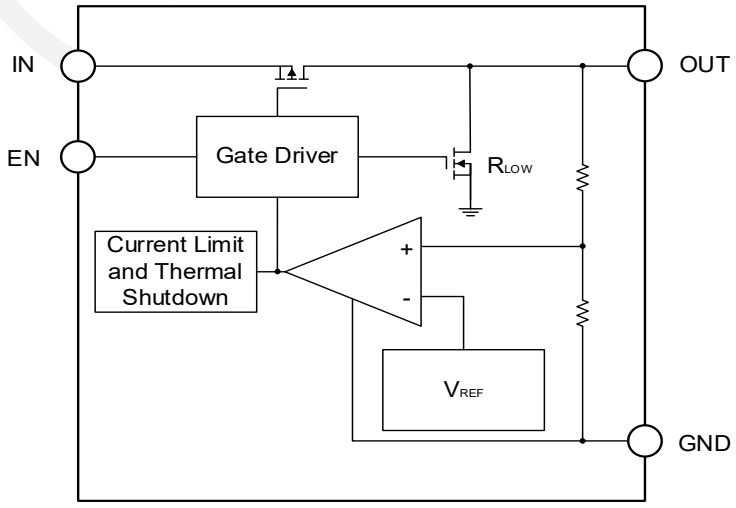


Figure2. Block Diagram

Functional Description

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins. With a reasonable PCB layout, the single 1μF ceramic output capacitor can be placed up to 10cm away from the CE53L8XX device.

Remote Output Capacitor Placement

The CE53L8XX requires at least a 1μF capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10cm away from the LDO.

ON/OFF Input Operation

The CE53L8XX is turned on by setting the EN pin higher than VIH threshold, and is turned off by pulling it lower than VIL threshold. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

Low Quiescent Current

The CE53L8XX, consuming only 20μA quiescent current, provides great power saving in portable and low power applications.

High PSRR and Low Noise

The CE53L8XX, with PSRR of 100dB at 1KHz,30mA is suitable for most of these applications that require high PSRR and low noise.

Fast Transient Response

The CE53L8XX's fast transient response from 0 to 400mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Dropout Voltage

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage. The CE53L8XX internal circuitry is not fully functional until V_{IN} is at least 2.2V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2V or (V_{OUT} + V_{DROP}).

Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuiting to GND, the current limit protection will be triggered and clamp the output current to approximately 650mA to prevent over-current and to protect the regulator from damage due to overheating.

Output Automatic Discharge

The CE53L8XX output employs an internal 350Ω (Typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

Thermal Overload Protection

Thermal shutdown disables the output when the junction temperature rises to approximately 150°C which allows the device to cool. When the junction temperature cools to approximately 120°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the CE53L8XX has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the CE53L8XX device into thermal shutdown may degrade device reliability

Absolute Maximum Ratings

Symbol	Parameters (Items)		Value	Unit
V_{IN}	Input Voltage (IN Pin)		-0.3 to 6.5	V
V_{EN}	Input Voltage (EN Pin)		-0.3 to 6.5	V
V_{OUT}	Output Voltage (OUT Pin)		-0.3 to V_{IN} + 0.3	V
P_{D_MAX}	Maximum Power Consumption		500	mW
I_{MAX}	Maximum Load Current		400	mA
T_J	Operating Junction Temperature		-40 to 150	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{SLOD}	Lead Temperature (Soldering, 10 sec)		260	°C
V_{ESD} (1)	ESD Classification	Human Body Model	±4000	V
		Charged Device Model	±1500	V
I_{LU} (1)	Latch Up Current Maximum Rating		±200	mA

Note2: This device series incorporates ESD protection and is tested by the following methods:

HBM tested per JEDEC JS-001;

CDM tested per JEDEC JS-002;

Latch up Current Maximum Rating tested per JEDEC JESD78F.

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V_{IN} (2)	Input Voltage	2.2 to 5.5	V
V_{OUT}	Output Voltage	1.2 to 4.3	V
I_{OUT}	Output Current	0 to 400	mA
T_A	Operating Ambient Temperature	-40 to 85	ºC
C_{IN}	Effective Input Ceramic Capacitor Value	0.68 to 10	μF
C_{OUT}	Effective Output Ceramic Capacitor Value	0.68 to 10	μF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Note3: In order to achieve high performance of PSRR, it is recommended that the V_{IN} needs to be no smaller than (V_{OUT} + 0.5V).

Electrical Characteristics

(V_{IN} = V_{OUT} + 1V, V_{EN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 1μF. T_A = 25°C, unless otherwise noted)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range (3)		2.2		5.5	V
V_{UVLO}	Under Voltage Lockout	V_{IN} Rising	1.8	2.0	2.2	V
		V_{IN} Falling	1.7	1.9	2.1	V
I_{Q_ON}	Input Quiescent Current	I_{OUT} = 0mA		20	40	uA
I_{Q_OFF}	Input Shutdown Quiescent Current	V_{EN} = 0V		0.1	1	uA
V_{OUT}	Output Voltage Accuracy	V_{IN} = $V_{OUT(NOM)}$ + 1V, I_{OUT} = 1mA, T_A = -40°C < T_A < 85°C	-1.5		1.5	%
Reg_{LINE}	Line Regulation	V_{IN} = V_{OUT} + 1V to 5.5V, I_{OUT} = 1mA		0.01	0.1	%/V
Reg_{LOAD}	Load Regulation	I_{OUT} = 1mA to 400mA		20	40	mV
V_{DROP}	Dropout Voltage (4)	V_{OUT} = 3.3V, I_{OUT} = 400mA		150	230	mV
		V_{OUT} = 3.6V, I_{OUT} = 400mA		140	220	mV
I_{OUT}	Output Current		400			mA
I_{LIMIT}	Current Limit	T_A = 25°C	450	650	850	mA
I_{SHORT}	Short Current Limit	V_{OUT} = 0V, T_A = 25°C	50	140	260	mA
PSRR	Power Supply Rejection Ratio (5)	f = 100Hz, I_{OUT} = 30mA		90		dB
		f = 1kHz, I_{OUT} = 30mA		100		dB
		f = 100kHz, I_{OUT} = 30mA		65		dB
		f = 1MHz, I_{OUT} = 30mA		45		dB
e_N	Output Noise Voltage (5)	BW = 10Hz to 100kHz, I_{OUT} = 10mA		9		μV_{RMS}
		BW = 10Hz to 100kHz, I_{OUT} = 200mA		8		μV_{RMS}
V_{IH}	EN Low Threshold	V_{IN} = 2.2V to 5.5V	0.84			V
V_{IL}	EN High Threshold	V_{IN} = 2.2V to 5.5V			0.40	V
I_{EN}	EN Input current	V_{EN} = 0V to 5.5V		0.5	1	uA
V_{TRLN}	Line Transient (5)	V_{IN} = (V_{OUT} + 1V) to (V_{OUT} + 2V) in 10us		5	20	mV
		V_{IN} = (V_{OUT} + 2V) to (V_{OUT} + 1V) in 10us		5	20	mV
V_{TRLD}	Load Transient (5)	I_{OUT} = 1mA to 400mA in 10us		25	60	mV
		I_{OUT} = 400mA to 1mA in 10us		20	45	mV
R_{LOW}	Output Discharge FET R_{dson}	V_{EN} = 0V, V_{IN} = 5V, I_{OUT} = 10mA	200	350	500	Ω
t_{ON}	Output Turn-on Time	From V_{EN} > V_{ENH} to V_{OUT} = 95% of $V_{OUT(NOM)}$		500		us
T_{TSD}	Thermal Shutdown Threshold (5)	T_J Rising		150		°C
T_{HYS}	Thermal Shutdown Hysteresis (5)	T_J Falling from Shutdown		30		°C

Note3: The maximum input voltage should take into account the maximum power consumption (P_{D_MAX}).

The calculation formula is as follows:

$$P_{D(MAX)} = (V_{IN(MAX)} - V_{OUT}) \times I_{OUT}$$

The maximum power consumption of the circuit is 500mW.

$$V_{IN(MAX)} = 500mW / I_{OUT} + V_{OUT}$$

For example:

If V_{OUT} = 1.2V, I_{OUT} = 400mA, the maximum input voltage is

$V_{IN(MAX)}$ = 500mW / 400mA + 1.2V = 2.45V

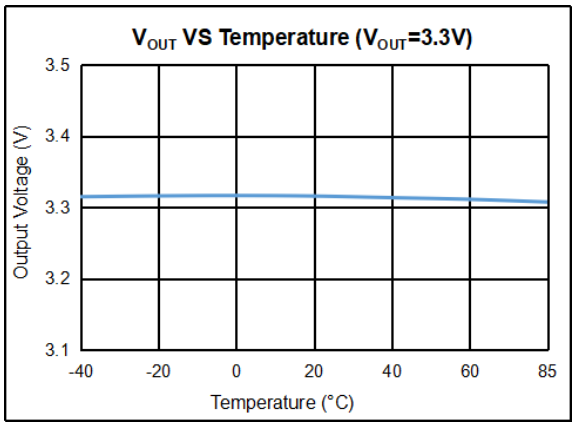
Note4: V_{DROP} FT test method: test the V_{OUT} voltage at V_{SET} + $V_{DROPMAX}$ with output current.

Note5: Guaranteed by design and characterization. Not a FT item.

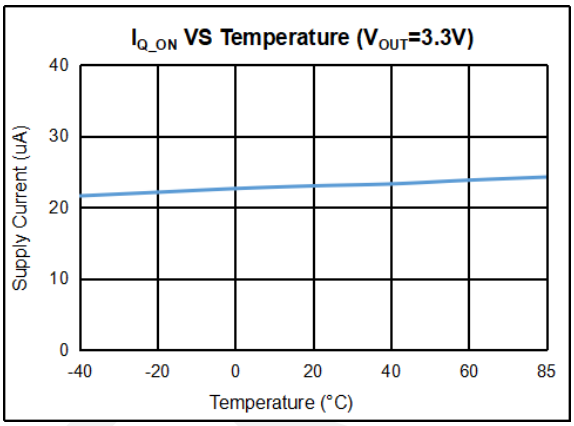
Typical Characteristics

VOLTAGE VERSION 3.3V

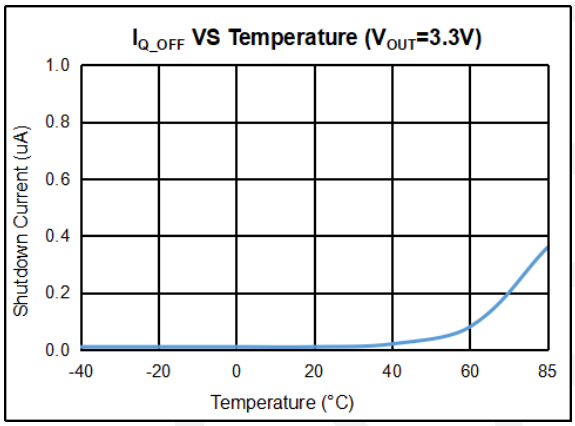
(V_{IN} = 4.3V, V_{EN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 1μF. T_A = 25°C, unless otherwise noted)



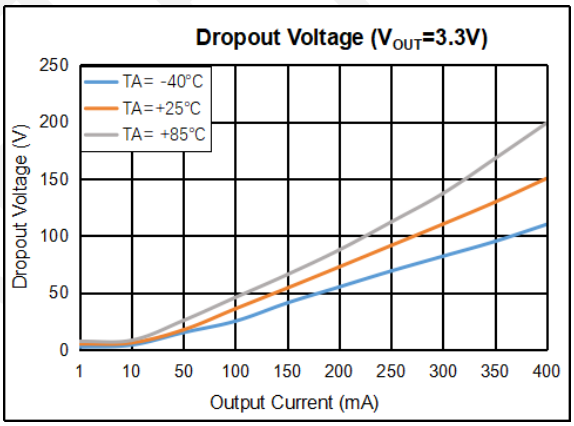
Output Voltage VS Temperature



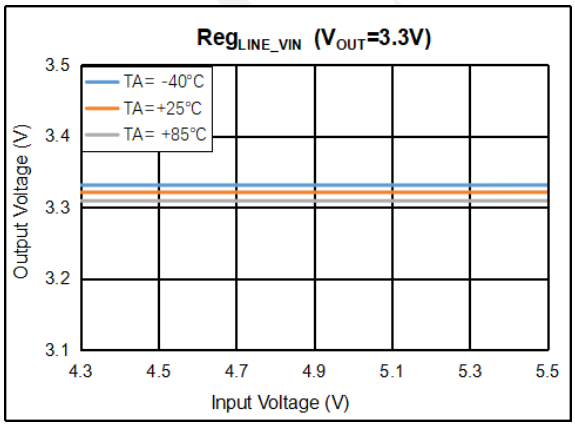
Supply Current VS Temperature



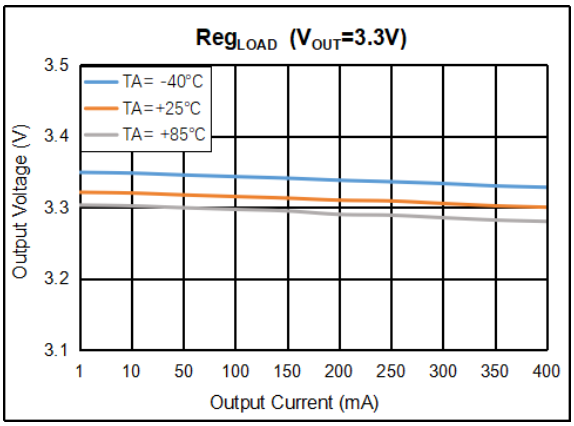
Shutdown Current VS Temperature



Dropout Voltage VS Output Current



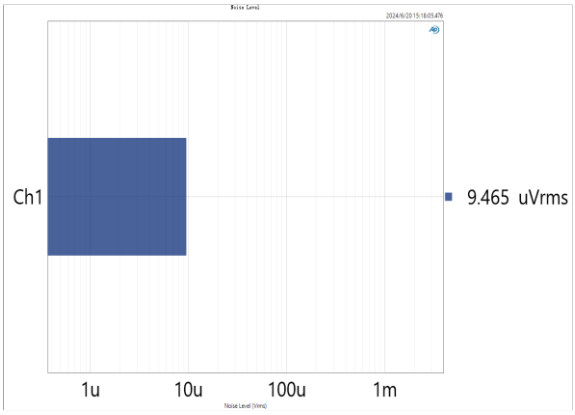
Output Voltage VS Input Voltage



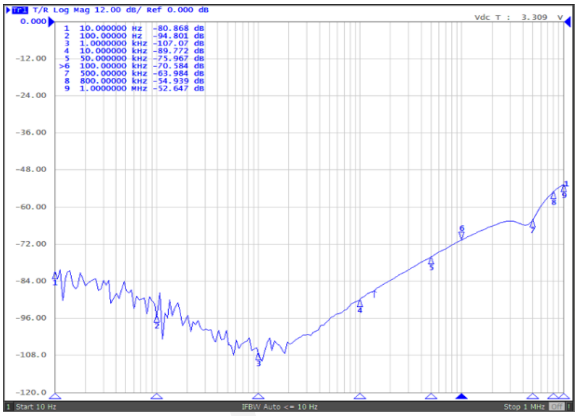
Output Voltage VS Output Current

Typical Characteristics (Continued)

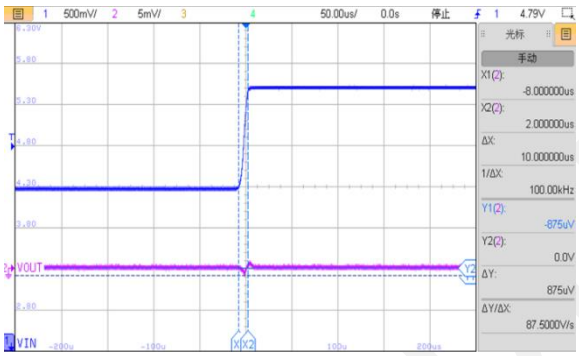
(V_{IN} = 4.3V, V_{EN} = 1.2V, I_{OUT} = 1mA, C_{IN} = 1μF, C_{OUT} = 1μF. T_A = 25°C, unless otherwise noted)



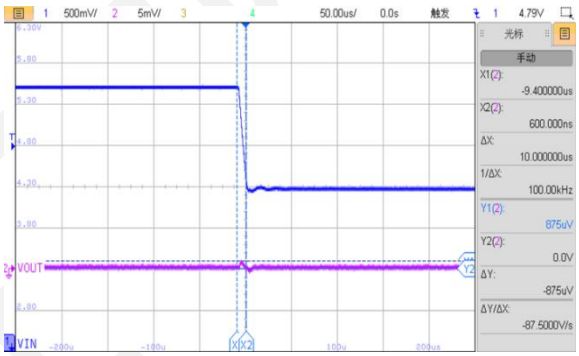
Noise (I_{OUT} = 200mA)



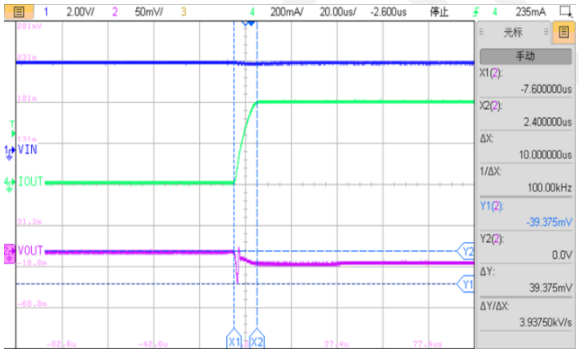
PSRR (I_{OUT} = 30mA)



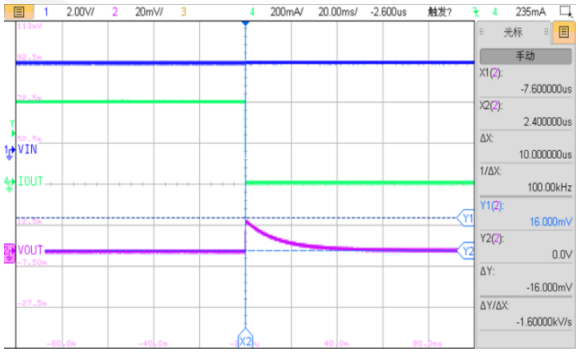
Line Transient (V_{IN} = 4.3~5.5V I_{OUT} = 1mA)



Line Transient (V_{IN} = 5.5~4.3V I_{OUT} = 1mA)



Load Transient (V_{IN} = 4.3V I_{OUT} = 1~400mA)



Load Transient (V_{IN} = 4.3V I_{OUT} = 400~1mA)

Application Circuits

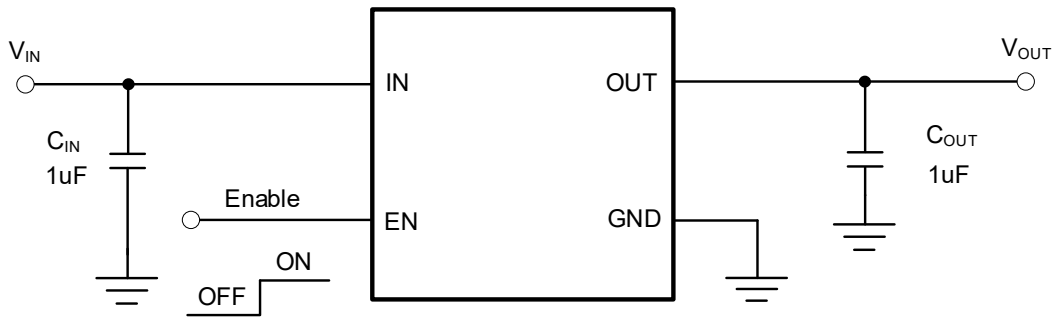


Figure3. Application Circuits

PCB Layout Guide

DFN4 (1mm × 1mm)

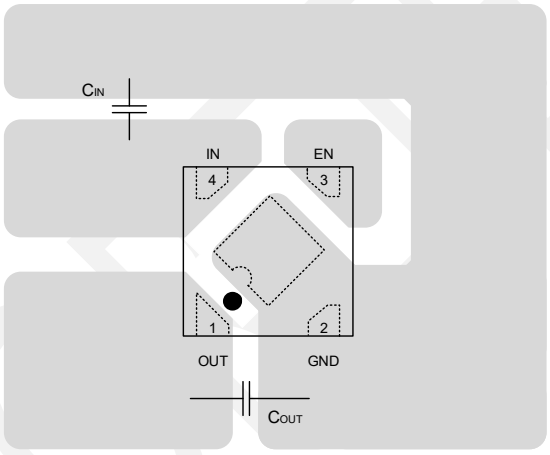


Figure4. PCB Layout Guide of DFN4

SOT23-5 (1.6mm × 2.9mm)

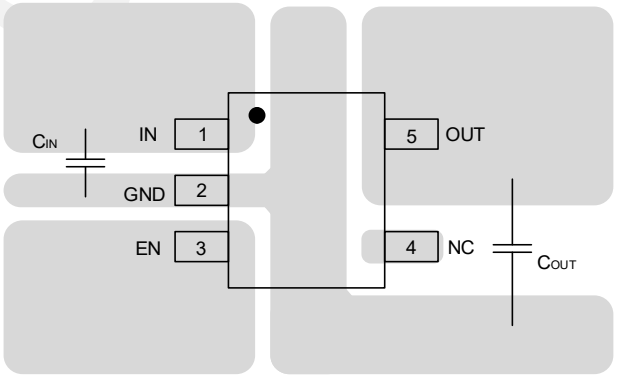
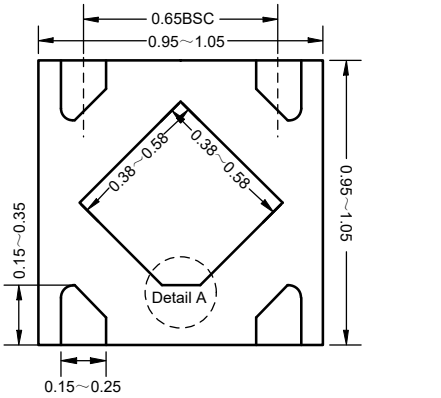
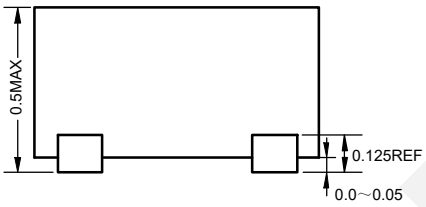


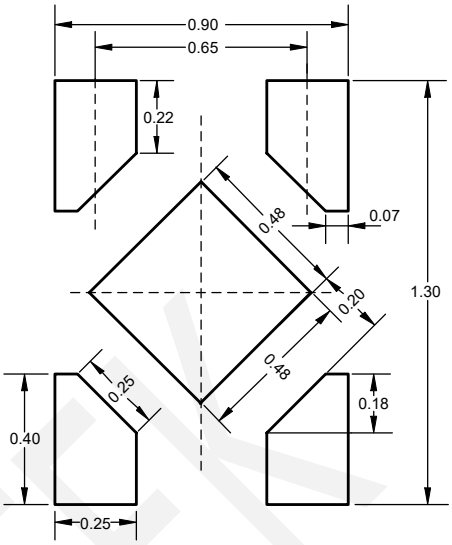
Figure5. PCB Layout Guide of SOT23-5

Package Dimension

DFN4 (1mm × 1mm)

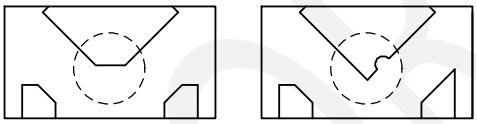






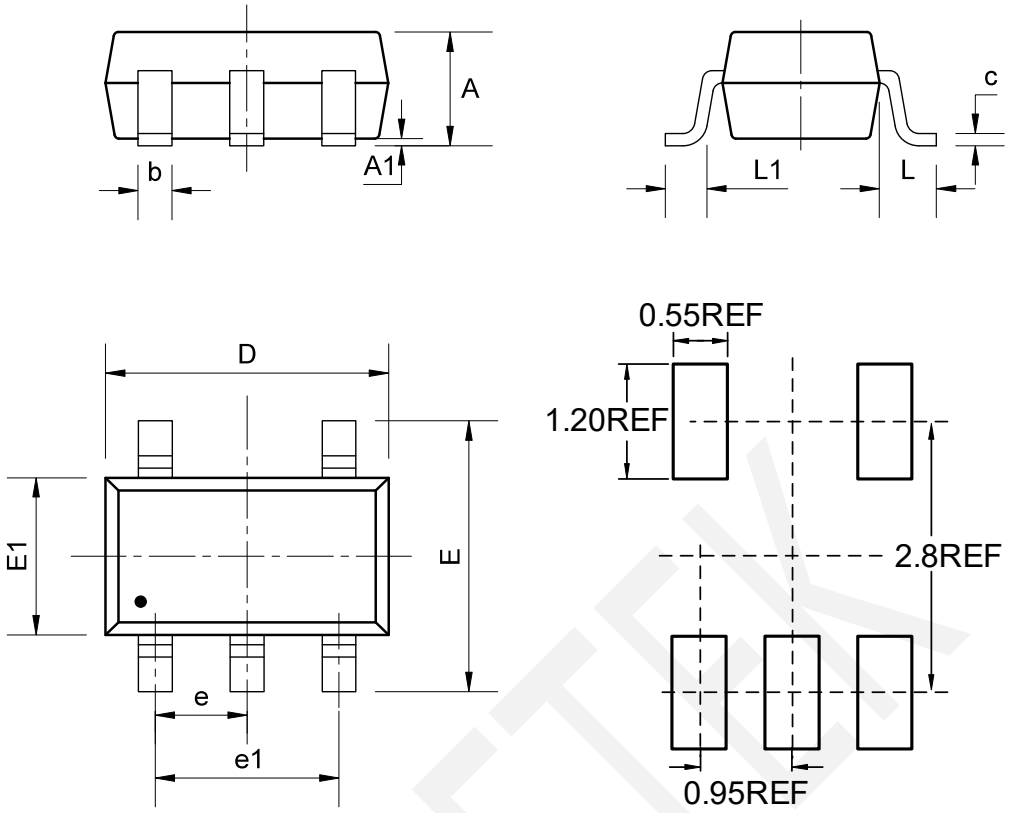
Recommended Land Pattern

Detail A: (PIN1 shape)



Unit: mm

SOT23-5 (1.6mm × 2.9mm)



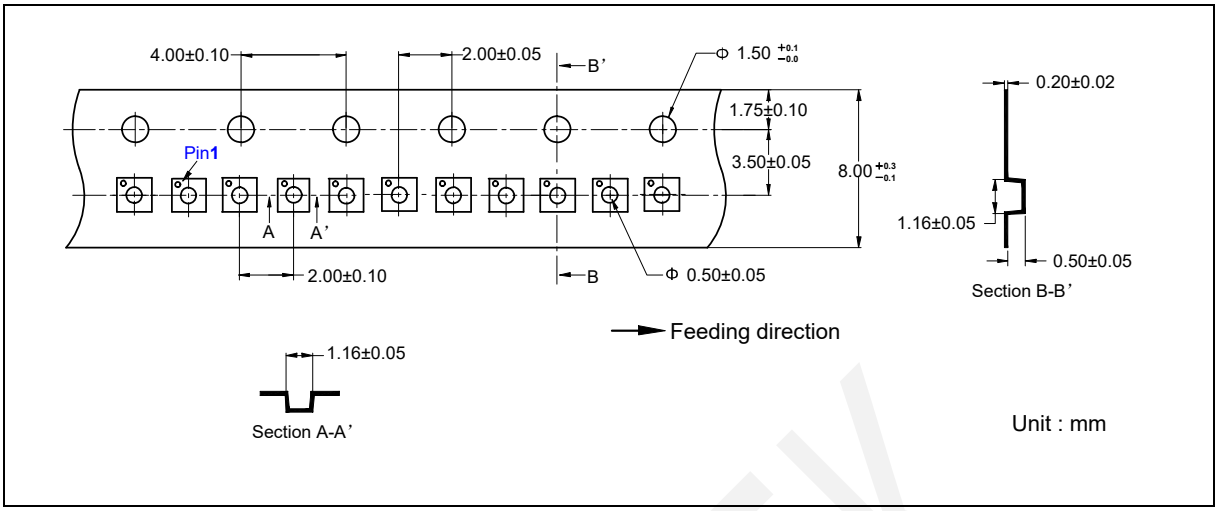
COMMON DIMENSIONS

(Unit: mm)

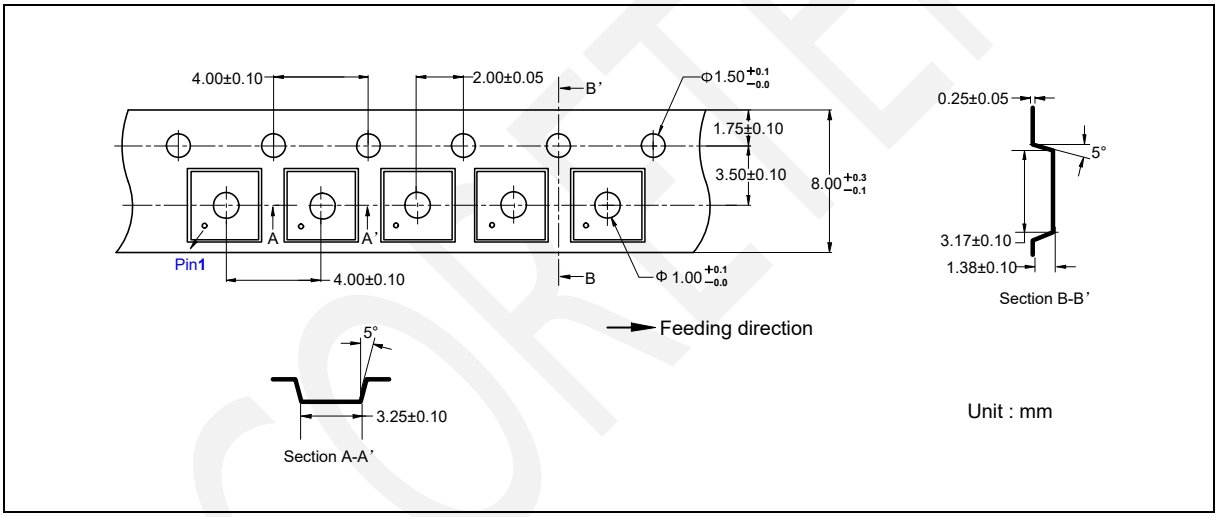
SYMBOL	MIN	NOM	MAX
A	-	-	1.45
A1	0.00	-	0.15
b	0.28	0.35	0.50
c	0.08	0.15	0.22
D	2.75	2.9	3.05
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
E	2.60	2.80	3.00
E1	1.45	1.6	1.75
L	0.60REF		
L1	0.30	0.45	0.60

Tape Information

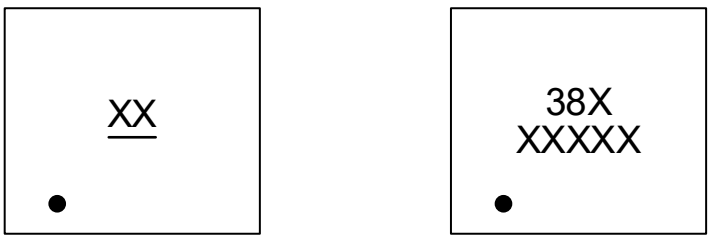
DFN4 (1mm × 1mm)



SOT23-5 (1.6mm × 2.9mm)



Marking Information



DFN4

$\underline{X}^{(1)}$ = Tracking Number

$\underline{X}^{(2)}$ = Output Version

SOT23-5

X = Output Version

XXXXX = Tracking Number

Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
0.0	2024-01-02	Preliminary Version	Li huan	Liu yihuo	Liu jiaying
1.0	2025-10-17	Official Version	Yang xiaoxu	Li huan	Liu jiaying