

CE53L1XX - 300mA Ultra-Low-Noise LDO

General Description

The CE53L1XX family of low-dropout (LDO), low-power linear regulators offer very high-power supply rejection ratio (PSRR) while maintaining very low 15 μ A ground current, suitable for RF applications. The family uses an advanced CMOS process and a PMOSFET pass device to achieve fast start-up, very low noise, excellent transient response and excellent PSRR performance.

The CE53L1XX is stable with a 1.0 μ F ceramic output capacitor, and uses a precision voltage reference and feedback loop to achieve a worst-case accuracy of 2% over all load, line, process and temperature variations. It is offered in a small DFN4 or SOT23-5 package, which is ideal for small form factor portable equipment such as wireless handsets.

Features

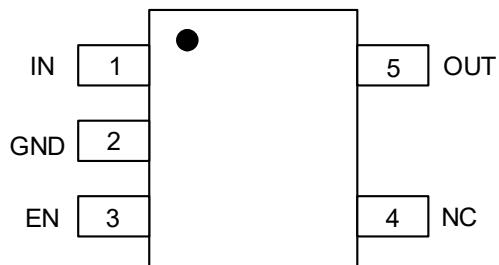
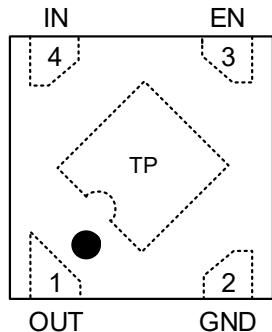
- Wide Input Voltage Range: 1.9V to 5.5V
- Up to 300mA Load Current
- Fixed Output Voltage Range: 1.2V~5.0V (1.2V, 1.5V, 1.6V, 1.8V, 2.2V, 2.5V, 2.8V, 3.0V, 3.1V, 3.3V and etc.)
- Other Output Voltage Options Available on Request
- Very Low Quiescent Current: 15 μ A Typical
- Low Dropout: 180mV typical@1.8V, 300mA
- Very High PSRR: 80db at 1KHz
- Ultra Low Noise: 10uVrms typical
- Excellent Load/Line Transient Response
- Excellent Load/Line Regulation
- With Auto Discharge Function
- Part No. and Package Information

Part No.	Package	Packing Option	MSL
CE53L1XXYB	DFN4 (1mm × 1mm)	Tape and Reel, 10K/Reel	1
CE53L1XX	SOT23-5 (1.6mm × 2.9mm)	Tape and Reel, 3K/Reel	3

Applications

- Smart Phones and Cellular Phones
- Smart Pad
- Digital Still Cameras
- Portable Instrument

Pin Configuration



DFN4(1mm × 1mm)

SOT23-5

Figure1. Pin Configuration

Pin Function

Pin No.		Pin Name	Pin Function
DFN4	SOT23-5		
1	5	OUT	Output Pin. A 1 μ F low-ESR capacitor should be connected to this pin to ground. An internal 50 Ω (typical) pull-down resistor prevents a charge remaining on OUT when the regulator is in the shutdown mode.
2	2	GND	Ground.
3	3	EN	Enable Control Input, active high. Do not leave EN floating.
4	1	IN	Supply Input Pin. Must be closely decoupled to GND with a 1 μ F or greater ceramic capacitor.
TP		Thermal Pad	Thermal Pad for DFN4(1x1) Package, Connect to GND or Leave Floating. Do not connect to any potential other than GND.
	4	NC	No connection.

Block Diagram

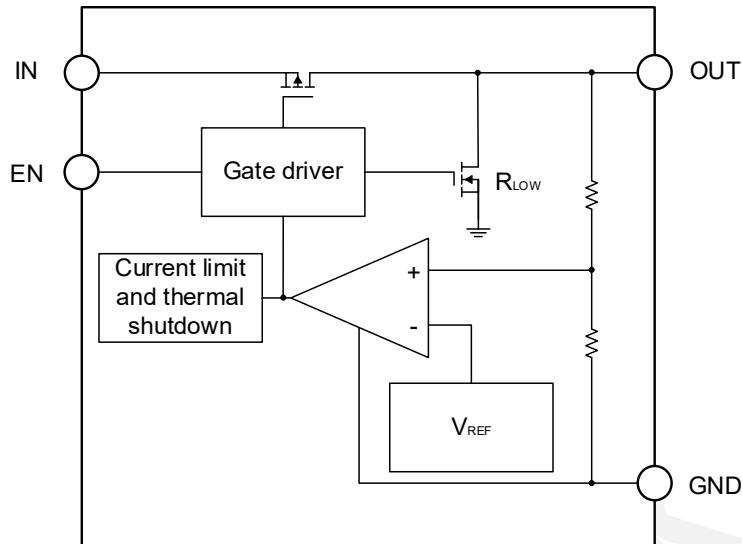


Figure2. Block Diagram

Functional Description

Input Capacitor

A $1\mu\text{F}$ ceramic capacitor is recommended to connect between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both IN and GND. The input capacitor should be at least equal to, or greater than, the output capacitor for good load transient performance.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is from $1\mu\text{F}$ to $10\mu\text{F}$, Equivalent Series Resistance (ESR) is from $5\text{m}\Omega$ to $100\text{m}\Omega$, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to OUT and GND pins. With a reasonable PCB layout, the single $1\mu\text{F}$ ceramic output capacitor can be placed up to 10cm away from the CE53L1XX device.

ON/OFF Input Operation

The CE53L1XX EN pin is internally held low by a $1\text{M}\Omega$ resistor to GND. The CE53L1XX is turned on by setting the EN pin higher than V_{IH} threshold, and is turned off by pulling it lower than V_{IL} threshold. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time.

High PSRR and Low Noise

The CE53L1XX, with PSRR of 80dB at 1KHz, is suitable for most of these applications that require high PSRR and low noise.

Output Automatic Discharge

The CE53L1XX output employs an internal 50Ω (typical) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

Remote Output Capacitor Placement

The CE53L1XX requires at least a $1\mu\text{F}$ capacitor at the OUT pin, but there are no strict requirements about the location of the capacitor in regards the OUT pin. In practical designs, the output capacitor may be located up to 10cm away from the LDO.

Fast Transient Response

The CE53L1XX's fast transient response from 0 to 300mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

Low Quiescent Current

The CE53L1XX, consuming only $15\mu\text{A}$ quiescent current, provides great power saving in portable and low power applications.

Minimum Operating Input Voltage (VIN)

The CE53L1XX does not include any dedicated UVLO circuitry. The CE53L1XX internal circuitry is not fully functional until VIN is at least 1.9V. The output voltage is not regulated until VIN has reached at least the greater of 1.9V or ($V_{\text{OUT}} + V_{\text{DROP}}$).

Current Limit Protection

When output current at the OUT pin is higher than current limit threshold or the OUT pin is short-circuiting to GND, the current limit protection will be triggered and clamp the output current to approximately 500mA to prevent over-current and to protect the regulator from damage due to overheating.

Thermal Overload Protection

Thermal shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 140°C , the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the CE53L1XX has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the CE53L1XX device into thermal shutdown may degrade device reliability.

Absolute Maximum Ratings

Symbol	Parameters (Items)	Value	Unit
V_{IN}	IN Pin Input Voltage	-0.3 to 6	V
V_{EN}	EN Pin Input Voltage	-0.3 to 6	V
V_{OUT}	OUT Pin Output Voltage	-0.3 to V_{IN} + 0.3	V
P_D	Maximum Power Consumption ⁽¹⁾	600	mW
I_{MAX}	Maximum Load Current	300	mA
T_J	Operating Junction Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-65 to 150	°C
T_{SLOD}	Lead Temperature (Soldering, 10 sec)	300	°C
V_{ESD}	Human Body Model per JEDEC JS-001	± 4000	V
	Charged Device Model per JEDEC JS-002	± 1500	V

Note1: Rating at mounting on a board (PCB board dimension: 40mm x 40mm (4layer), copper: 1OZ).

Recommended Operating Conditions

Symbol	Parameters	Rating	Unit
V_{IN}	Input Voltage	1.9 to 5.5	V
I_{OUT}	Output Current	0 to 300	mA
T_A	Operating Ambient Temperature	-40 to 85	°C
C_{IN}	Effective Input Ceramic Capacitor Value	0.47 to 10	µF
C_{OUT}	Effective Output Ceramic Capacitor Value	0.47 to 10	µF
ESR	Input and Output Capacitor Equivalent Series Resistance	5 to 100	mΩ

Electrical Characteristics

($V_{IN} = V_{OUT} + 1V$, $V_{EN} = 1.2V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $T_A = 25^\circ C$, unless otherwise noted)

Symbol	Parameters	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range		1.9		5.5	V
V_{OUT}	Output Voltage Range		1.2		5.0	V
ΔV_{OUT}	Output Voltage Tolerance	$V_{IN} = (V_{OUT(NOM)} + 1V)$ to 5.5V $I_{OUT} = 1mA$ to 300mA	-2		2	%
$Line_{REG}$	Line Regulation	$V_{IN} = (V_{OUT} + 1V)$ to 5.5V, $I_{OUT} = 1mA$		0.02		%/V
$Load_{REG}$	Load Regulation	$I_{OUT} = 1mA$ to 300mA		15	40	mV
I_{LOAD}	Load Current		300			mA
I_{Q_OFF}	Input Shutdown Quiescent Current	$V_{EN} = 0V$		0.2	1	uA
I_{Q_ON}	Input Quiescent Current /Channel	$V_{EN} = 1.2V$, $V_{IN} = V_{OUT} + 1V$ $I_{OUT} = 0mA$		15	25	uA
		$V_{EN} = 1.2V$, $V_{IN} = V_{OUT} + 1V$ $I_{OUT} = 300mA$		250	425	uA
V_{DROP}	Dropout Voltage	$V_{OUT} = 1.2V$, $I_{OUT} = 300mA$			700	mV
		$V_{OUT} = 1.8V$, $I_{OUT} = 300mA$		180		mV
		$V_{OUT} = 2.8V$, $I_{OUT} = 300mA$		135		mV
		$V_{OUT} = 3.3V$, $I_{OUT} = 300mA$		110		mV
I_{LIMIT}	Current Limit	$R_{LOAD} = 1\Omega$, $T_A = 25^\circ C$	400	600	1000	mA
I_{SHORT}	Short Current Limit	$V_{OUT} = 0V$, $T_A = 25^\circ C$		60		mA
$PSRR^{(2)}$	Power Supply Rejection Ratio	$f = 100Hz$, $I_{OUT} = 20mA$		80		dB
		$f = 1kHz$, $I_{OUT} = 20mA$		80		dB
		$f = 10kHz$, $I_{OUT} = 20mA$		65		dB
		$f = 100kHz$, $I_{OUT} = 20mA$		40		dB
$e_N^{(2)}$	Output Noise Voltage	$BW = 10Hz$ to $100kHz$, $I_{OUT} = 1mA$		10		μV_{RMS}
		$BW = 10Hz$ to $100kHz$, $I_{OUT} = 300mA$		6.5		μV_{RMS}
R_{LOW}	Output Discharge FET R_{dson}	$V_{EN} = 0V$, $I_{OUT} = 10mA$		50		Ω
V_{IL}	EN Input Logic Low Voltage	$V_{IN} = 1.9V$ to 5.5V, V_{EN} Falling until the Output is Disabled			0.4	V
V_{IH}	EN Input Logic High Voltage	$V_{IN} = 1.9V$ to 5.5V, V_{EN} Rising until the Output is Enabled	1.2			V
I_{EN}	EN Input Leakage Current	$V_{IN} = 5.5V$, $V_{EN} = 0V$		0.01	1	uA
		$V_{IN} = 5.5V$, $V_{EN} = 5.5V$		5.5		uA

Electrical Characteristics (Continued)

($V_{IN} = V_{OUT} + 1V$, $V_{EN} = 1.2V$, $I_{OUT} = 1mA$, $C_{IN} = 1\mu F$, $C_{OUT} = 1\mu F$, $T_A = 25^\circ C$, unless otherwise stated)

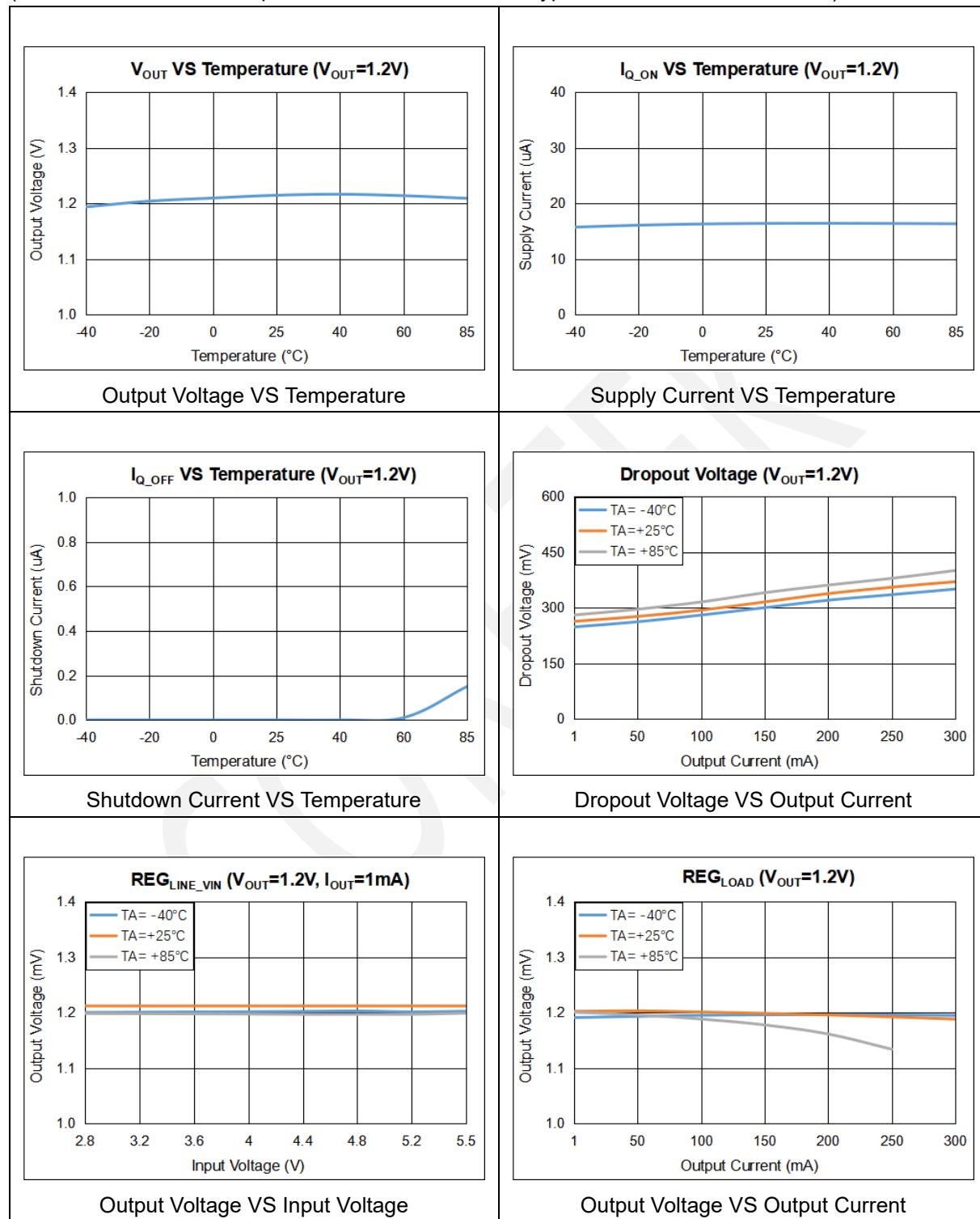
Symbol	Parameters	Conditions	Min	Typ	Max	Unit
$\Delta V_{OUT}^{(2)}$	Line Transient	$V_{IN} = (V_{OUT} + 1V)$ to $(V_{OUT} + 1.6V)$ in 10us		10		mV
		$V_{IN} = (V_{OUT} + 1.6V)$ to $(V_{OUT} + 1V)$ in 10us		10		mV
	Load Transient	$I_{OUT} = 1mA$ to $300mA$ in 10us		30		mV
		$I_{OUT} = 300mA$ to $1mA$ in 10us		30		mV
	Overshoot on Start-Up	Stated as Percentage of $V_{OUT(NOM)}$			5	%
t_{ON}	Output Turn-On Time	From $V_{EN} > V_{IH}$ to $V_{OUT} = 95\%$ of $V_{OUT(NOM)}$		70	150	us
T_{SHDN}	Thermal Shutdown Threshold ⁽²⁾	T_J Rising		160		°C
T_{HYS}	Thermal Shutdown Hysteresis ⁽²⁾	T_J Falling from Shutdown		15		°C

Note2: Guaranteed by design and characterization. not a FT item.

Typical Characteristics

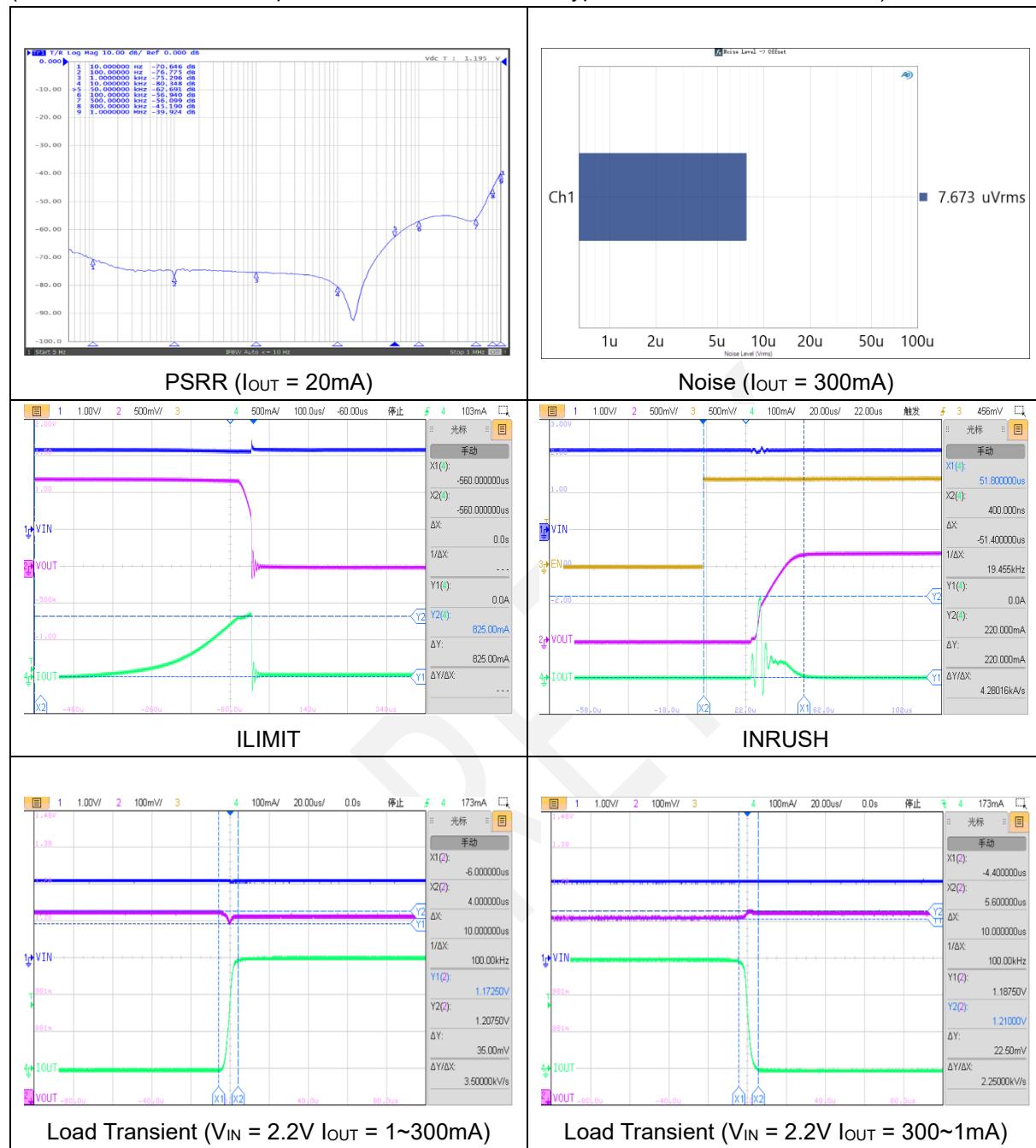
VOLTAGE VERSION 1.2V

($V_{IN} = 2.2V$; $C_{IN} = C_{OUT} = 1\mu F$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)



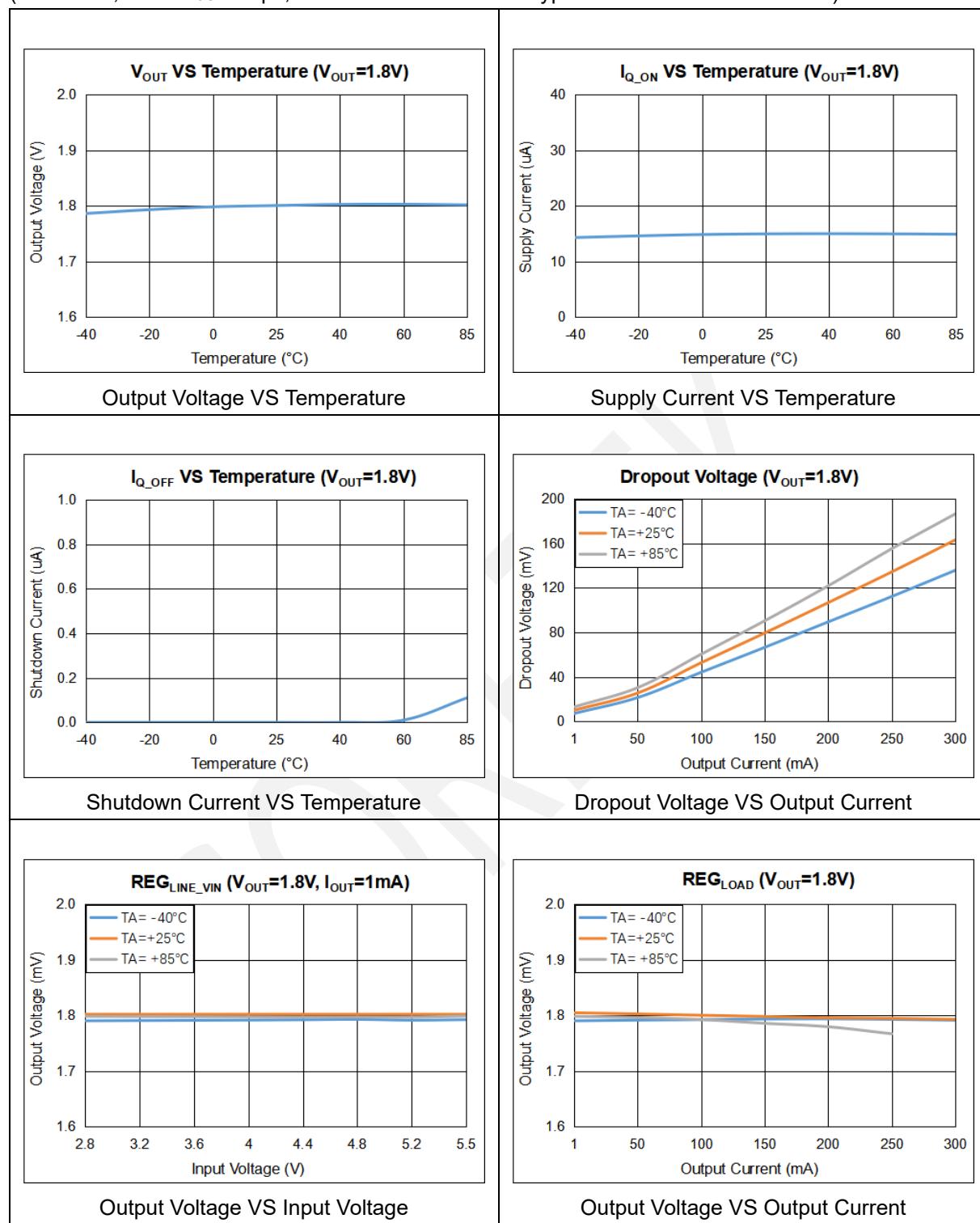
VOLTAGE VERSION 1.2V

($V_{IN} = 2.2V$; $C_{IN} = C_{OUT} = 1\mu F$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)



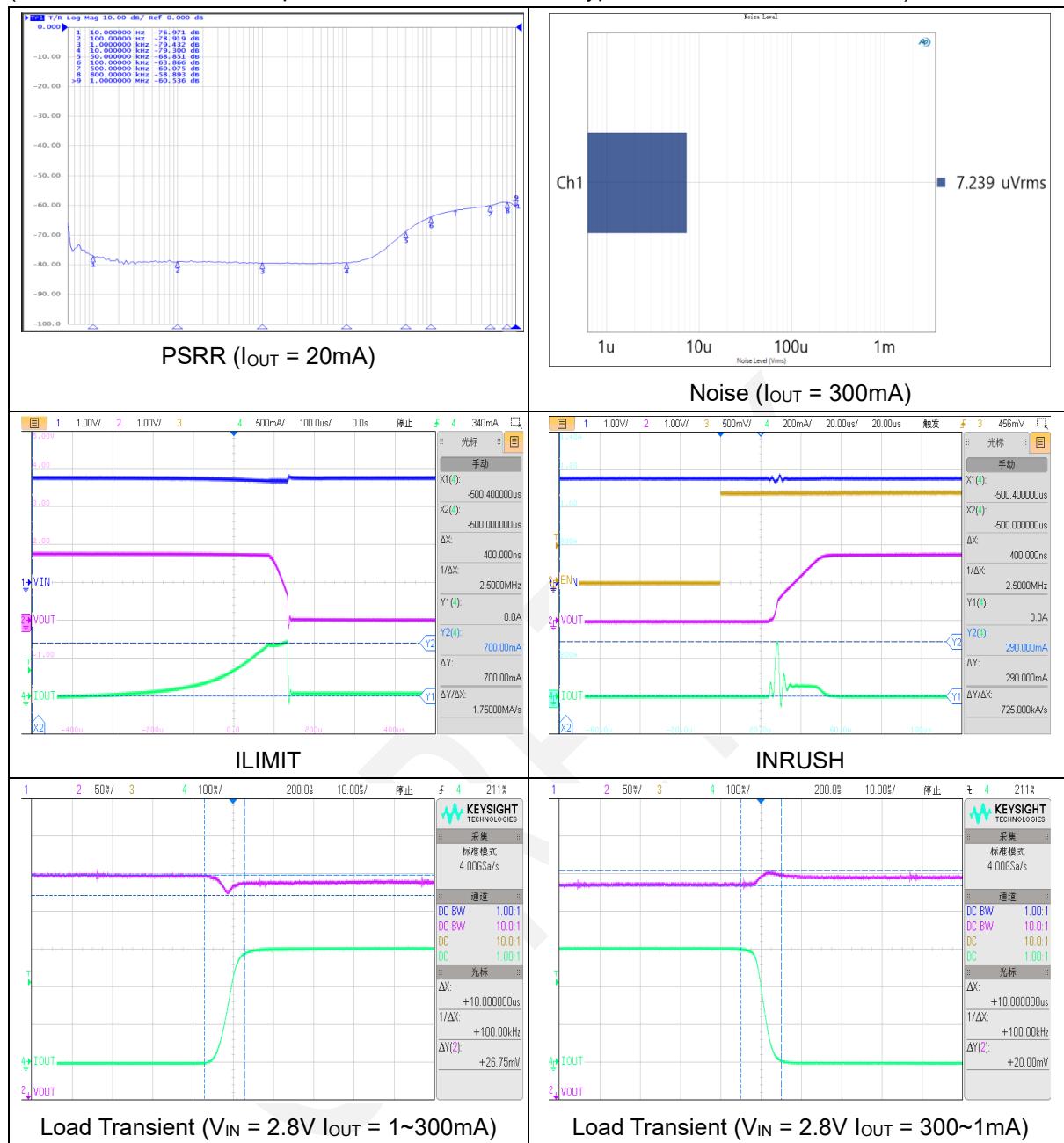
VOLTAGE VERSION 1.8V

($V_{IN} = 2.8V$; $C_{IN} = C_{OUT} = 1\mu F$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)



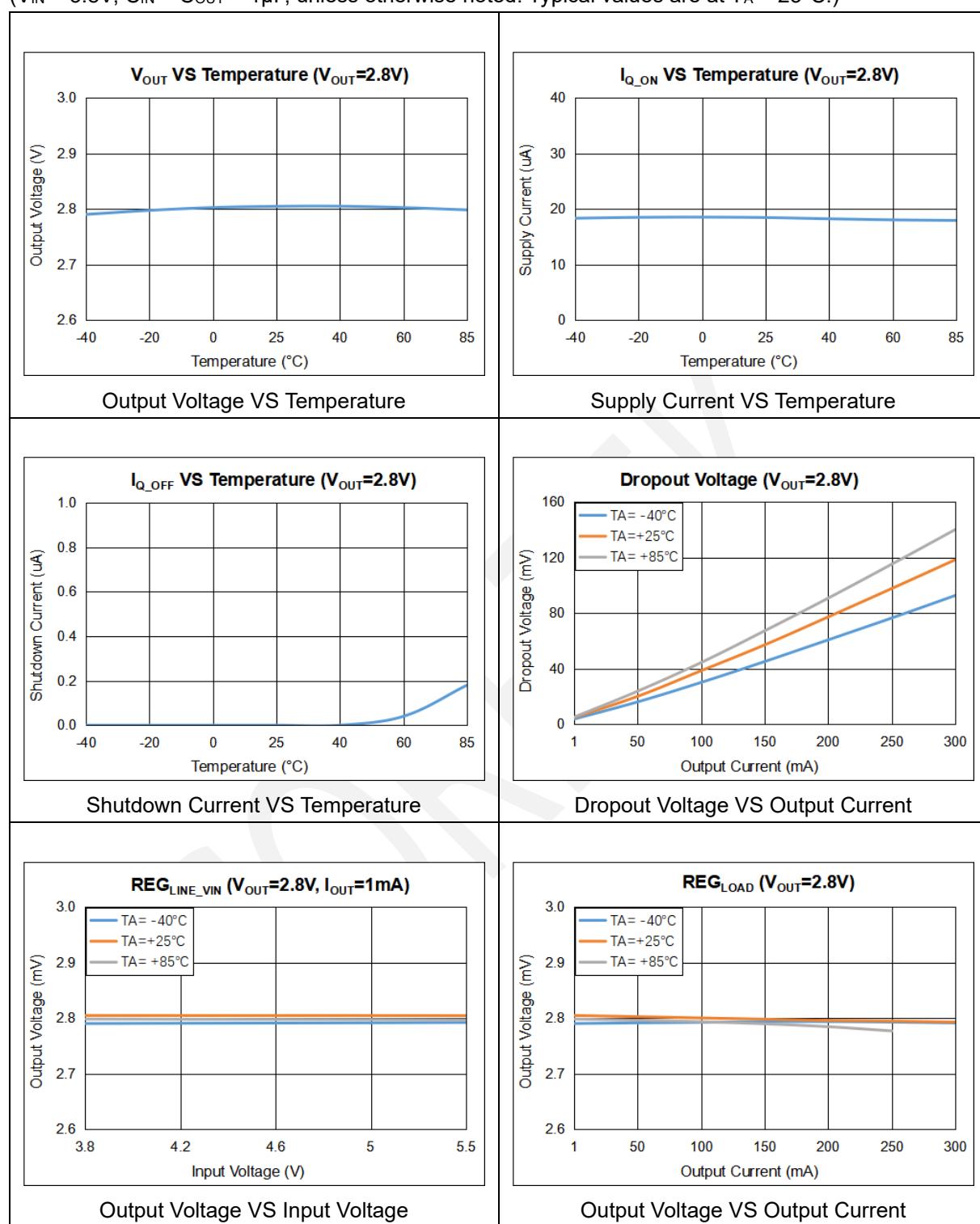
VOLTAGE VERSION 1.8V

($V_{IN} = 2.8V$; $C_{IN} = C_{OUT} = 1\mu F$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)



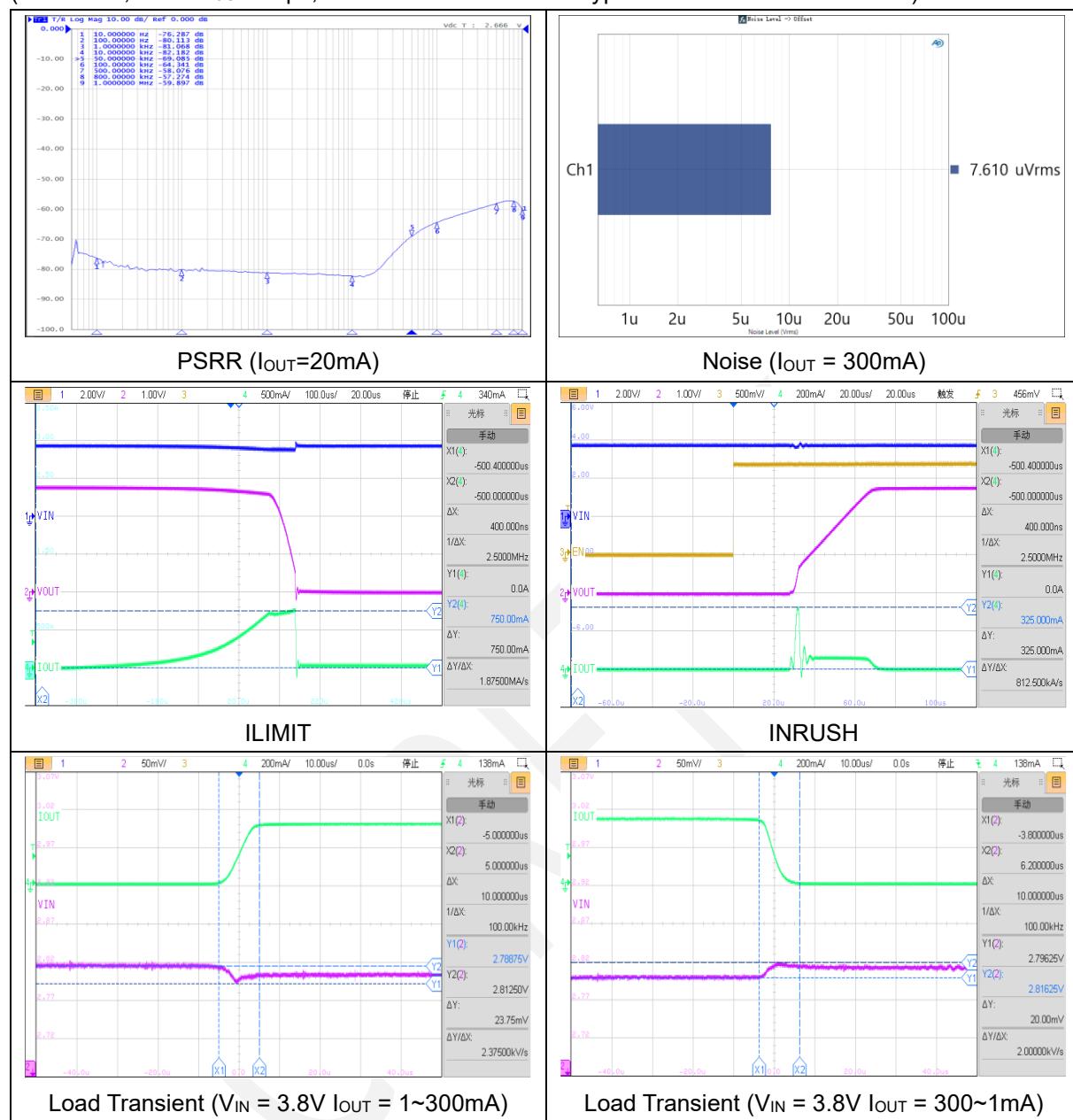
VOLTAGE VERSION 2.8V

($V_{IN} = 3.8V$; $C_{IN} = C_{OUT} = 1\mu F$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)



VOLTAGE VERSION 2.8V

($V_{IN} = 3.8V$; $C_{IN} = C_{OUT} = 1\mu F$, unless otherwise noted. Typical values are at $T_A = 25^{\circ}C$.)



Application Circuits

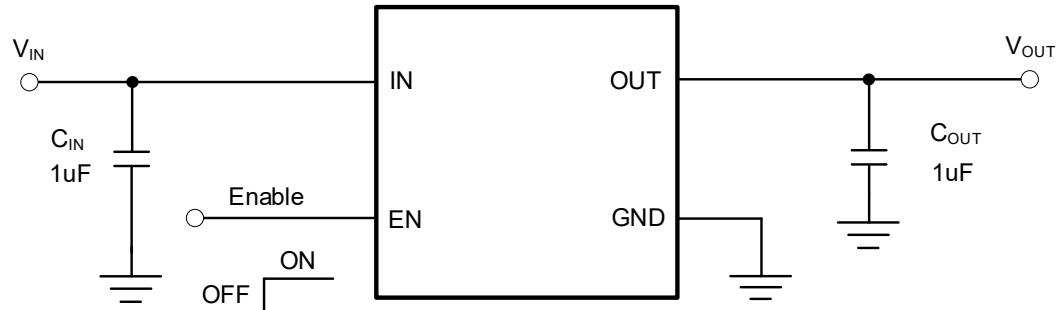


Figure3. Application Circuits

PCB Layout Guide

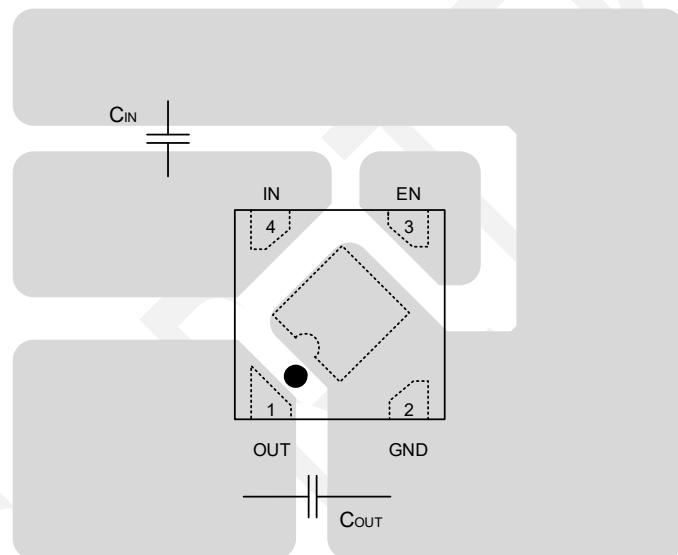


Figure4. PCB Layout Guide of DFN4

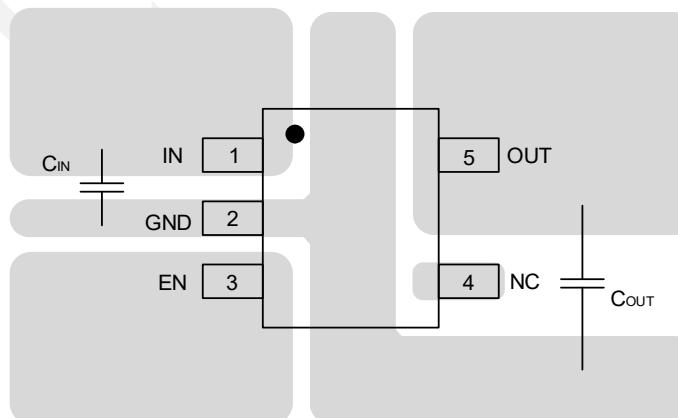
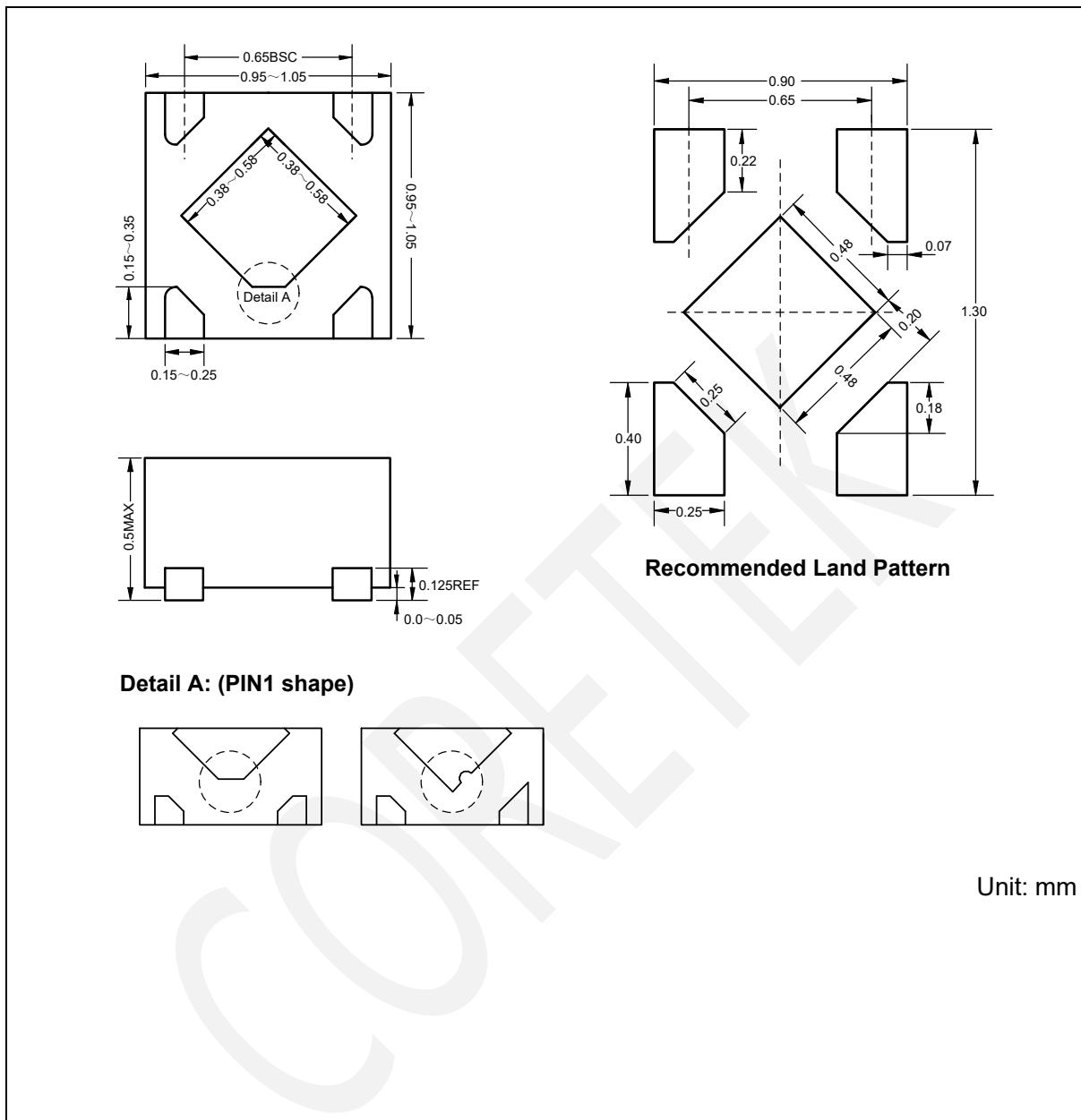


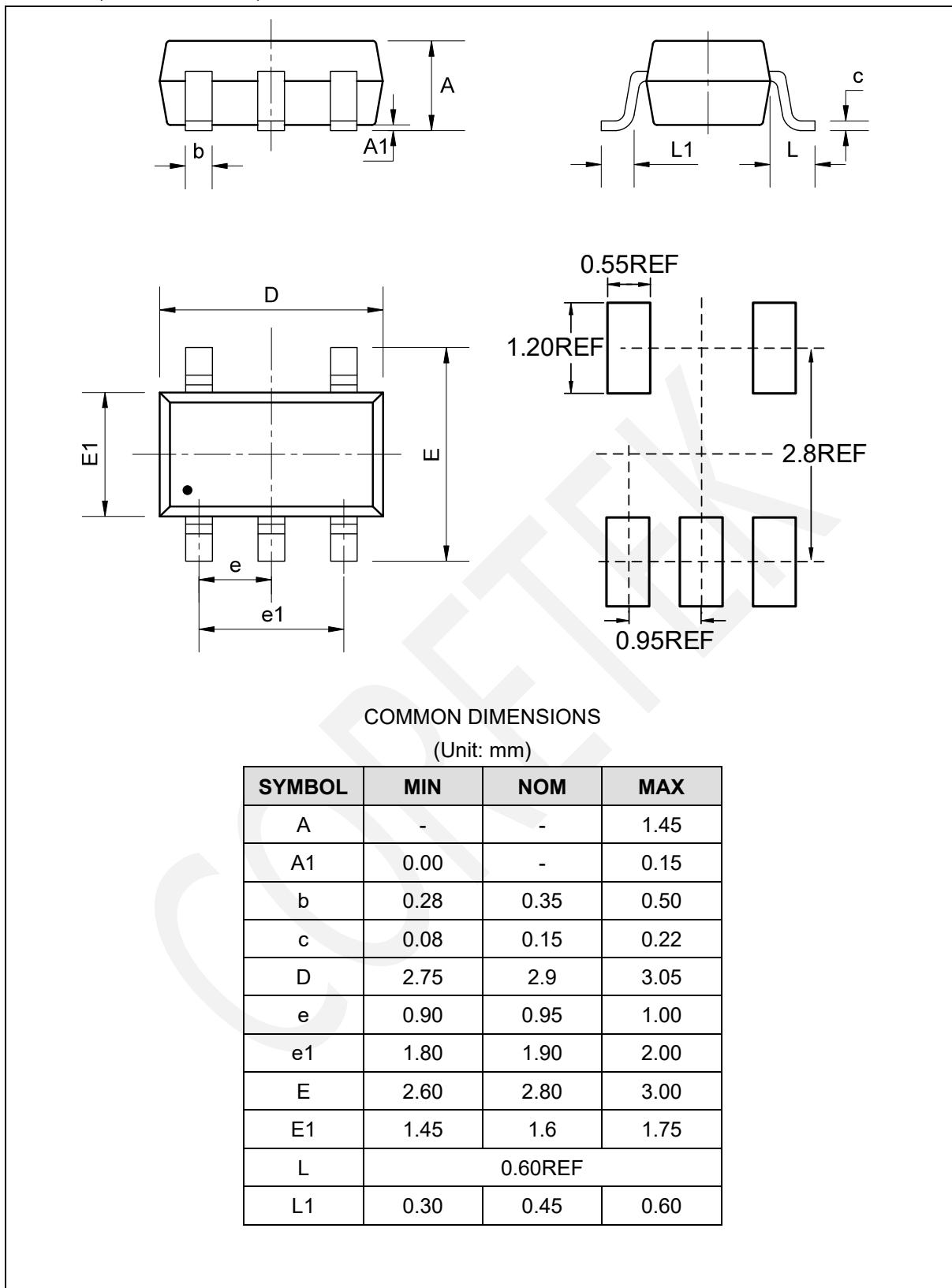
Figure5. PCB Layout Guide of SOT23-5

Package Dimension

DFN4 (1mm x 1mm)

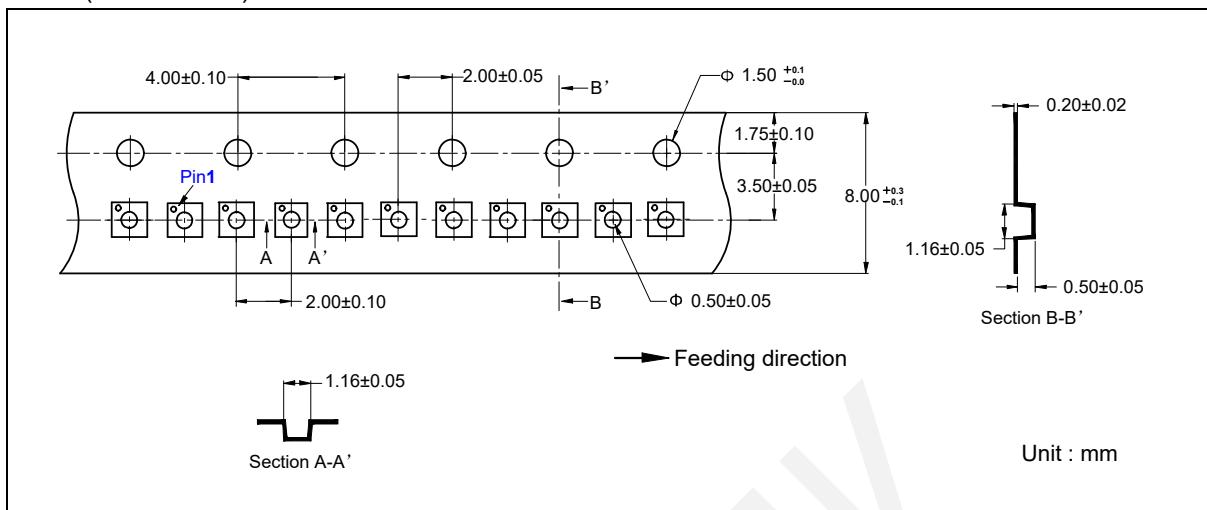


SOT23-5 (1.6mm x 2.9mm)

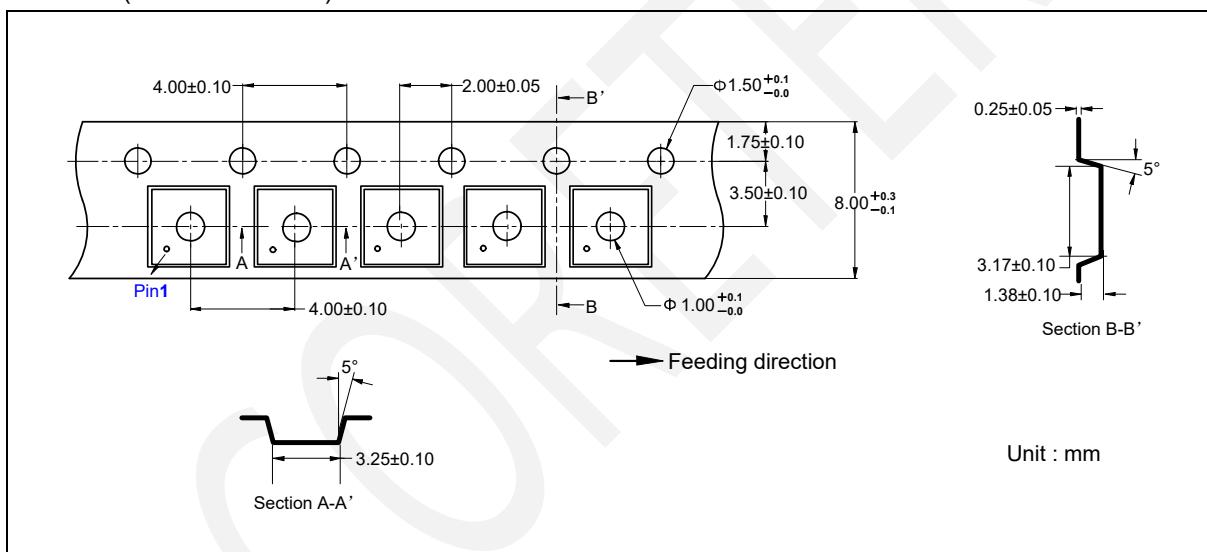


Tape Information

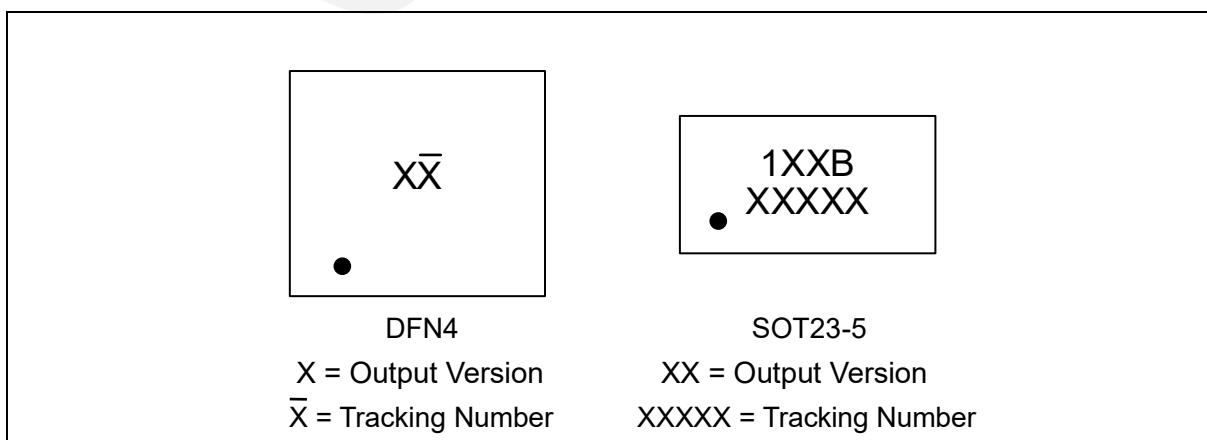
DFN4 (1mm × 1mm)



SOT23-5 (1.6mm × 2.9mm)



Marking Information



Revision History and Checking Table

Version	Date	Revision Item	Modifier	Function & Spec Checking	Package & Tape Checking
1.0	2018-06-27	Original Version	Liu yiguo	Liu yiguo	Liu jiaying
1.1	2018-12-12	Update EC Table	Liu yiguo	Liu yiguo	Liu jiaying
1.2	2022-08-24	Update Typeset	Yang xiaoxu	Liu yiguo	Yang xiaoxu
1.3	2023-10-11	Update Package Picture	Shi bo	Liu yiguo	Yang xiaoxu
1.4	2025-09-09	Update Characteristic Diagram	Shi bo	Liu yiguo	Yang Xiao Xu
1.5	2025-10-09	Update Device information	Shi bo	Liu yiguo	Liu jiaying